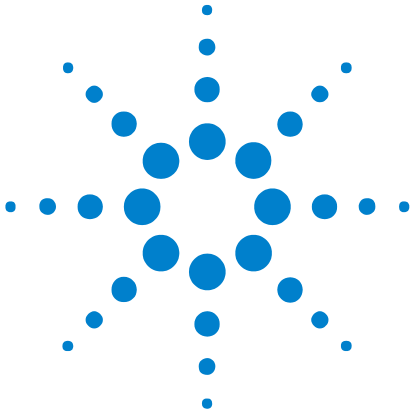

U4301A PCIe Gen3 Analyzer

User Guide

Agilent Technologies

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U4301A PCIe Gen3 Analyzer—At a Glance

The U4301A PCIe Gen3 analyzer lets you capture and decode PCI Express 3.0 (PCIe 3.0) data and view it in a Packet Viewer/Protocol Viewer window. The protocol analyzer supports all PCIe 3.0 speeds, including 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2) through PCIe 8 GT/s (Gen3), and it supports link widths from x1 to x16.

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2 slot chassis).

When a controller PC is connected to an Agilent Digital Test Console chassis via an external PCIe interface and cable, the *Agilent Logic Analyzer* application (running on the controller PC) lets you connect to the chassis, set up U4301A PCIe Gen3 analyzer data captures, and perform analysis.

The U4301A PCIe Gen3 analyzer provides:

Effective presentation of protocol interactions from physical layer to transaction layer:

- Industry standard spreadsheet format protocol viewer with:
  - Highlighting by packet type or direction.
  - Easy flow columns to better understand the stimulus and response nature of the protocols.
  - Context sensitive columns to show only the relevant information, minimizing the need to scroll horizontally.
- Flexible GUI configuration to meet debug needs, with pre-defined GUI layouts for Link Training debug, Config accesses, and general I/O.

Simple and powerful state-based triggering:

- New simple trigger mode makes it easy to setup single event triggers.
- Powerful state-based triggering including:
  - Four states supported in trigger sequencer.
  - Triggering on patterns (ordered set patterns or packet types).
  - Internal counters and timers.
  - Triggering on an ordered set on a specific lane.
- External trigger in/out.

Powerful hardware features ensure capture of important transition events:

- Dual phase lock loops (PLLs) per direction ensuring that the analyzer will lock on speed change events quickly and not miss any critical data.
- Large 4 GB of capture buffer per module (up to 8 GB of capture for x16 analyzer), for long recording sessions.

- PCIe Gen1 x4 link to the host PC, provides up to 10 Gbps of data download.
- LEDs to show lane status and speed for fast understanding of current link status.

See • "Using the PCIe Gen3 Analyzer" on page 5

Using the PCIe Gen3 Analyzer

For an overview and list of features, see: "U4301A PCIe Gen3 Analyzer–At a Glance" on page 3

- Chapter 1, “Hardware and Software Installation,” starting on page 9
- Chapter 2, “Probing Options for PCIe Gen3,” starting on page 11
- Chapter 3, “Specifying the Connection Setup,” starting on page 13
- Chapter 4, “Setting the Capture Options,” starting on page 25
- Chapter 5, “Tuning the Analyzer for a Specific DUT,” starting on page 29
- Chapter 7, “Setting Up Triggers,” starting on page 57
- Chapter 8, “Running/Stopping Captures,” starting on page 67
- Chapter 9, “Viewing PCIe Gen3 Packets,” starting on page 69

See Also

- U4305 PCIe Gen3 exerciser documentation.

Contents

1 Hardware and Software Installation

The U4301A PCIe Gen3 analyzer is a module installed in an Agilent Digital Test Console chassis (for example, the U4002A portable 2-slot chassis) or Agilent AXIe chassis (for example, the M9502A 2-slot chassis).

The Agilent chassis is connected to a controller PC via a PCI Express interface and cable.

The controller PC runs the *Agilent Logic Analyzer* application software which lets you set up the U4301A PCIe Gen3 analyzer, specify triggers and other data capture options, capture data, and analyze the captured data using Packet Viewer/Protocol Viewer windows.

See the *"Agilent Digital Test Console Installation Guide"* for information on:

- Installing the U4301A PCIe Gen3 analyzer blade into a Digital Test Console chassis.
- Connecting the Digital Test Console chassis to a controller PC via the PCI Express Gen1 x4 interface.
- Installing the *Agilent Logic Analyzer* software on the controller PC.

See the "*Agilent AXIe based Logic Analysis and Protocol Test Modules Installation Guide*" for information on:

- Installing the U4301A PCIe Gen3 analyzer module into an Agilent AXIe chassis.
- Connecting the AXIe chassis to a controller PC via the PCI Express interface.
- Installing the Agilent Logic Analyzer software on the controller PC.

2 Probing Options for PCIe Gen3

The currently available options for probing a PCIe Gen3 device under test (DUT) are:

- U4321A solid slot interposer
- U4322A midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

Details about these two probing options (and other PCIe Gen3 tools) can be found in the *"PCI Express Gen3 Hardware and Probing Guide"*.

3 Specifying the Connection Setup

Once you have connected the U4301A module, probing hardware, and DUT in the required configuration based on your probing requirements, the next step is to configure the connection setup for the U4301A module in the Agilent Logic Analyzer application. You use the Connection Setup tab of the analyzer's Setup dialog to configure the connection setup.

The connection setup details that you specify in this tab tells the Logic Analyzer software how the U4301A module is connected to the DUT in terms such as the probing option used, the direction of data capture (upstream, downstream, or bidirectional), and the link width needed. For instance, if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the Footprint option, 1 Bidirectional upto x8 as the Link type, and x8 as the Link Width in the Connection Setup tab to reflect the hardware setup that you have configured.

NOTE

- For details on how to set up the hardware and probing connections between the U4301A module and DUT, refer to PCI Express Gen3 Hardware and Probing Guide.
- For details on how to set up the chassis, U4301A module, and host PC, refer to the AXIe based Logic Analysis and Protocol Test Modules Installation Guide.

These guides are installed with the Logic Analyzer software and can also be downloaded from www.agilent.com.

Probing options

While specifying the connection setup, one of the key requirements is to select the probing option that you have used with the U4301A module to probe the DUT and the data capture direction in which you have configured the hardware setup.

Broadly, there are the following four probing options available with the U4301A module:

- U4321A Solid Slot Interposer card
- U4322A Soft Touch Midbus 3.0 probe
- U4324A PCIe Gen3 Flying Lead probe

- PCIe Gen2 probes with the U4317A adapter. This adapter is used for conversion between the PCIe Gen2 probes and U4301A PCIe Gen3 Analyzer module. The PCIe Gen2 probes supported are:
  - N5315A Solid Slot Interposer for PCIe Gen2
  - N4241A straight, N4242A swizzled, and N4243A split cable Soft Touch Midbus 2.0 probe for PCIe Gen2
  - N5328A Half Size Midbus probe
  - N4241F/Z Flying Lead probe for PCIe Gen2

For each of the above four probing types, different options are available in the Connection Setup tab reflecting the data direction (upstream, downstream, or bidirectional). Upstream is the data direction towards the root complex. Downstream is the data direction away from the root complex. Based on your probing setup and the data capture direction in which you have configured the hardware setup, you need to select an appropriate probing option in the Connection Setup tab.

U4321A Solid Slot Interposer Card

When used with a U4321A solid slot interposer card, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way.

If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and a U4321A SSI card. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select U4321A Slot Interposer Upstream as the probing option for one of the U4301A modules and U4321A Slot Interposer Downstream as the probing option for the other U4301A module.

if you have connected the U4301A module hardware to the DUT using the U4321A Solid Slot Interposer card in a x8 bidirectional setup, then you need to select the U4321 Slot Interposer Both Dir x8 as the probing option.

U4322A Soft Touch Midbus 3.0 probe

The U4322A midbus 3.0 probes require footprints to be designed into the device under test. Each probe requires its own footprint, and there are basically two variations:

- **Bidirectional** – where half the footprint pins are for the upstream data and the other half are for the downstream data.
- **Unidirectional** – where all the pins on the footprint are for the data going in the same direction.

Reversed refers to optional lane reversal which is supported for upstream ports.

Based on how you have designed the footprint for the probe, you need to select an appropriate probing option in the Connection Setup tab. For instance, if you have configured a x4 bidirectional setup using a U4322A midbus probe, then you need to select U4322A Bidirectional Full as the Footprint, 1 Bidirectional upto x8 as the Link type, and x4 as the Link Width in the Connection Setup tab.

U4324A PCIe Gen 3 Flying Lead probe

When used with a U4324A Flying Lead probe, one U4301A module can probe in the upstream (x1-x16), downstream (x1-x16), or bidirectional (x1-x8) way. For x1-x8 bidirectional link type, you can use the U4324A Flying Lead probes in a straight or a swizzled configuration.

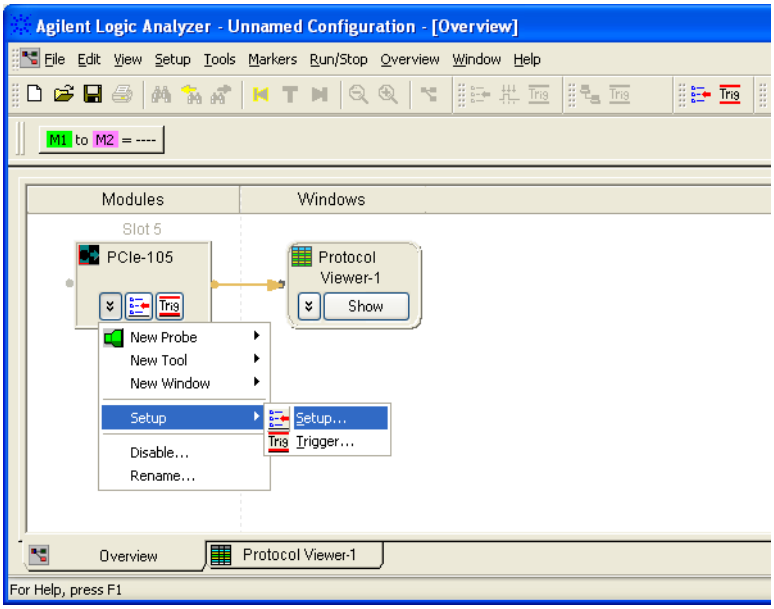
If you need to probe in both upstream as well downstream directions with a x16 link width, you need two U4301A Analyzer modules and eight U4324A Flying Lead probes. To reflect such a hardware setup in the Connection Setup tab of the Logic Analyzer application, you need to select the U4324A Flying Lead Probe as the probing option and Unidirectional as the link type for both the U4301A modules.

If you have connected the U4324A Flying Lead probes in a x1 to x8 bidirectional straight setup, then you need to select the U4324A Flying Lead Probe as the probing option and Bidirectional as the link type.

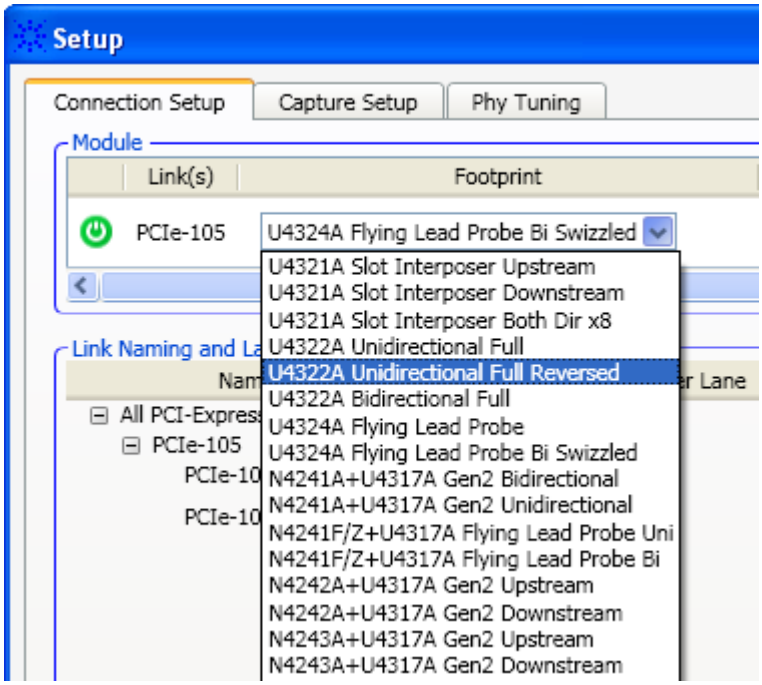
If you have set up a swizzled x1 to x8 bidirectional configuration using the U4324A Flying Lead probes, then you need to select the U4324A Flying Lead Probe Bi Swizzled as the probing option and Bidirectional as the link type.

To specify the connection setup

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Setup...**.

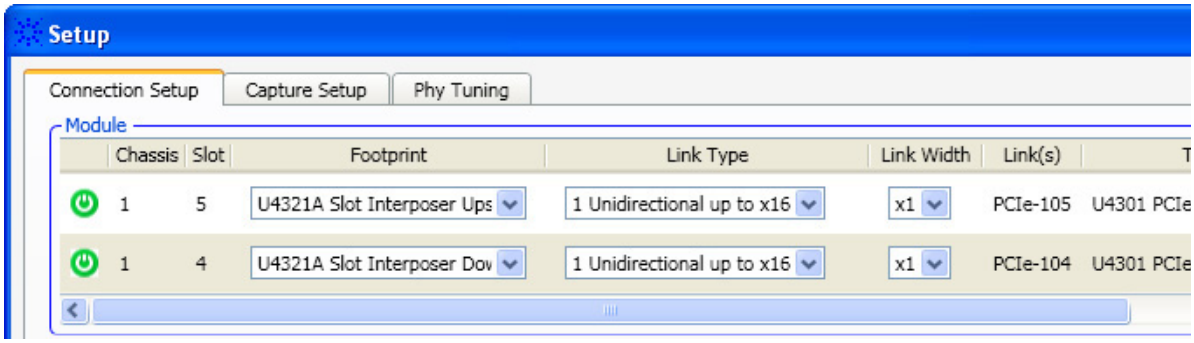


2 From the **Footprint** listbox, select the type of probing that you have set up between the U4301A Analyzer module and DUT. For each of the supported four probing types, different probing options are available in the Footprints listbox based on the data direction (upstream, downstream, or bidirectional). Based on your probing setup and the link type needed, select an appropriate probing option from the Footprint listbox. Refer to the "Probing options" on page 13 to know more about these options.

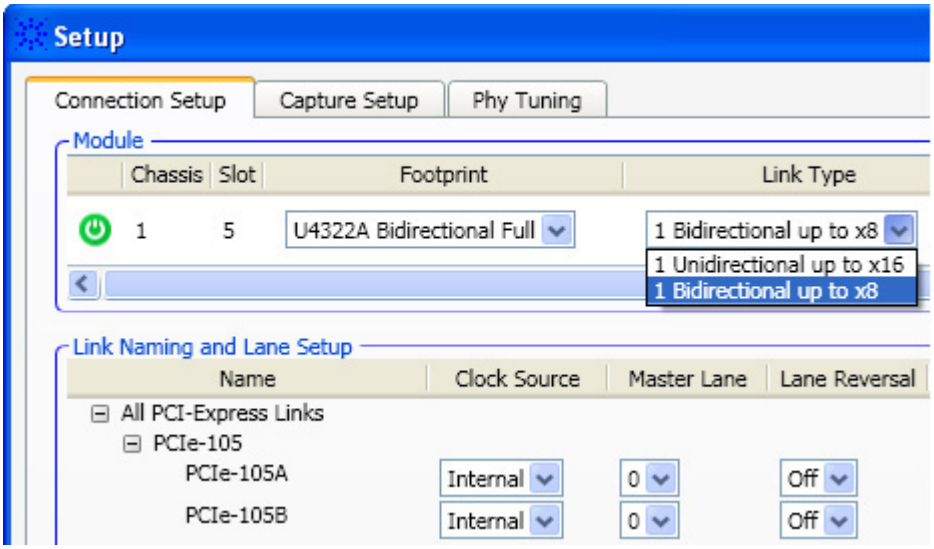


For more information on probing setups, click **Connection diagram...** or refer to the *"PCI Express Gen3 Hardware and Probing Guide"*.

If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the probing option individually for these modules.

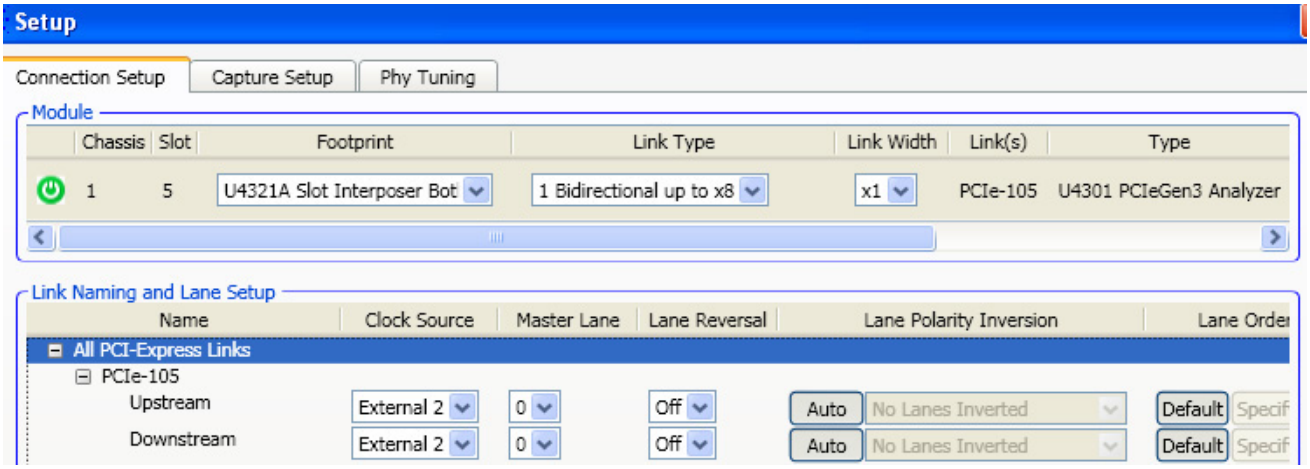


3 Specify the link type.



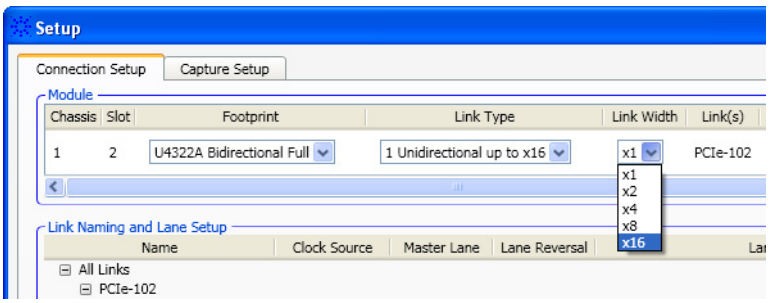
The **Link Type** refers to the type of link that you want to create between the U4301A module and DUT. You can select the **1 Unidirectional up to x16** link type if you want the U4301A module to probe and capture data in only one direction (upstream or downstream). In the Unidirectional link type, the U4301A module can support a unidirectional link with upto 16 channels in the same direction. You can select the **1 Bidirectional up to x8** link type if you want the same U4301A module to probe and capture data in both directions (upstream as well as downstream). In the bidirectional link type, the U4301A module can support one bidirectional link with upto eight channels for each direction. When you select the bidirectional link type, two sub-links are created for the two directions. You can set the link attributes such as clock source, master lane, and lane ordering separately for these two sub-links. These attributes are available in the **Link Naming and Lane Setup** section.

The following screen displays the sub-links of a x8 bidirectional link. These sub-links have been renamed on the basis of the direction these represent.



If you have installed multiple U4301A modules in the chassis, all these modules are listed in the Module section of the tab. You need to select the link type individually for these modules.

4 Select the link width.

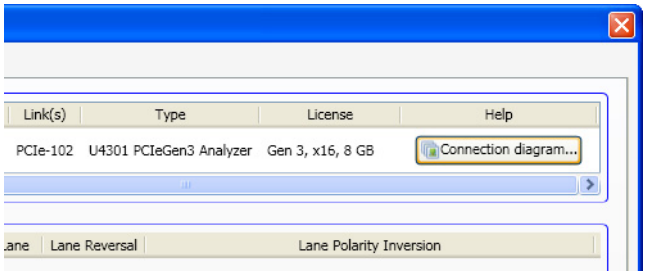


Select the link width that matches the negotiated link width of transmitter and receiver.

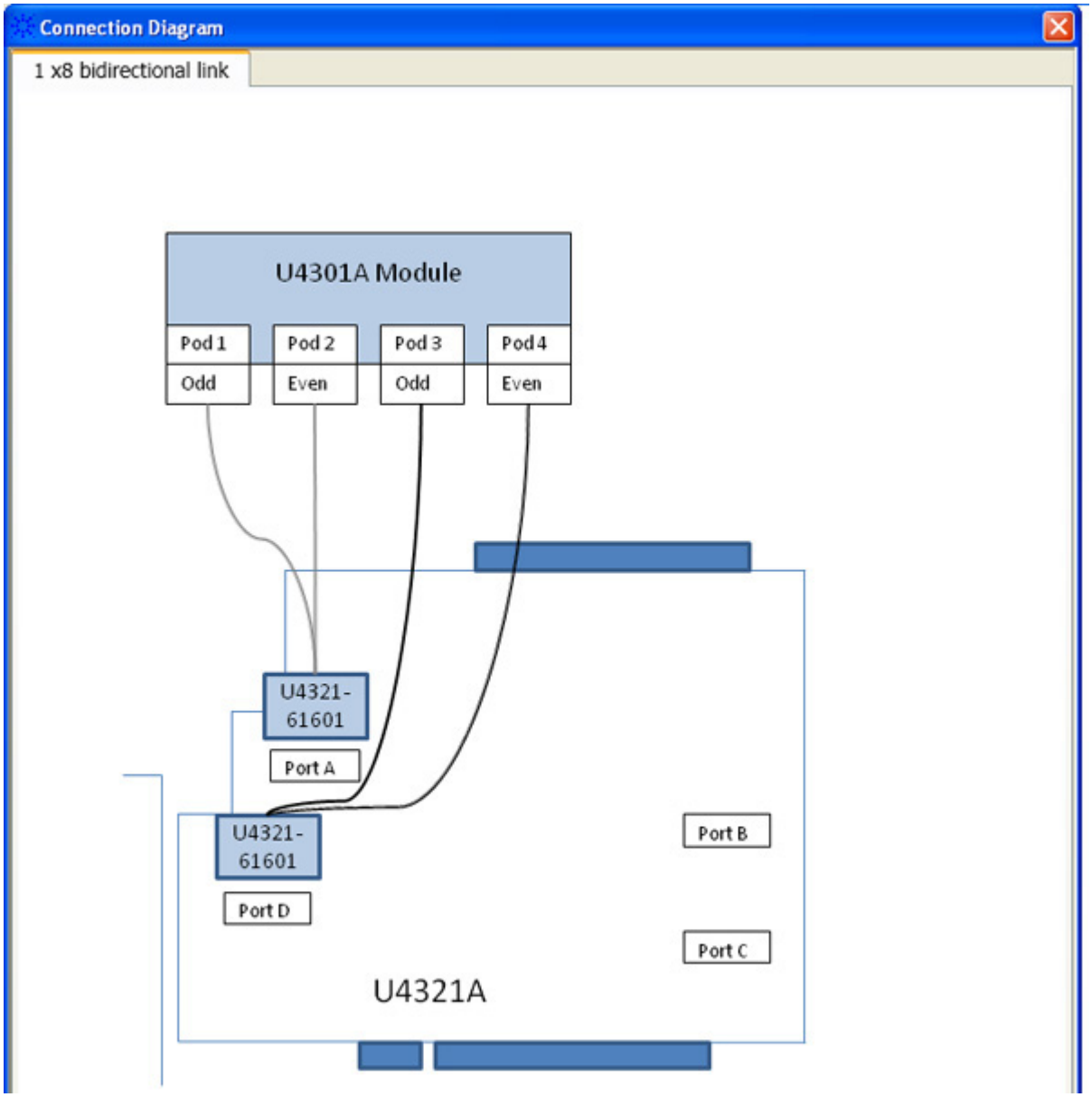
If you select the Link Type as **1 Bidirectional upto x8**, then you can select the Link Width from x1 to x8. The x16 option is disabled in this case because a U4301A Analyzer module can probe and capture data in both directions with upto eight channels in each direction.

5 Verify the connection:

a Click **Connection diagram...**.

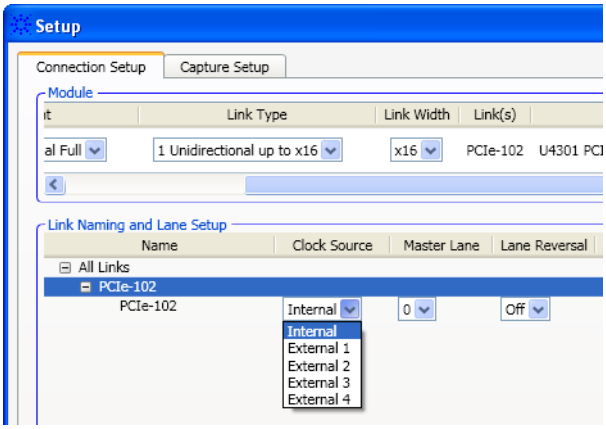


b Use the Connection Diagram dialog to verify that your connection setup specification matches the actual device under test connection.



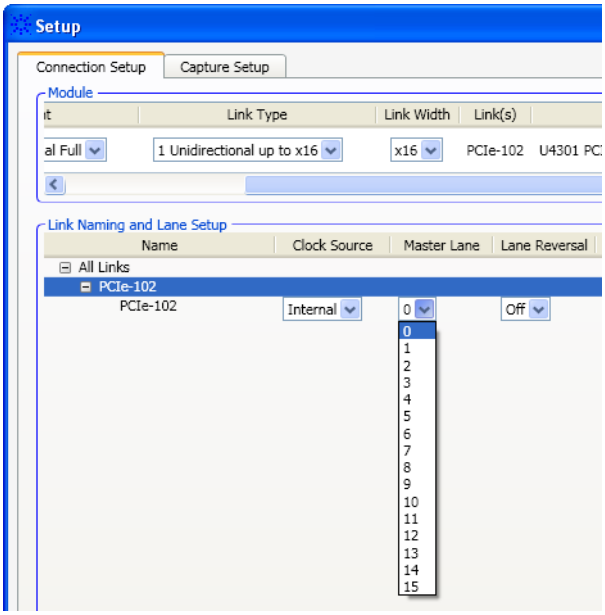
c Close the Connection Diagram dialog.

6 Select the clock source:

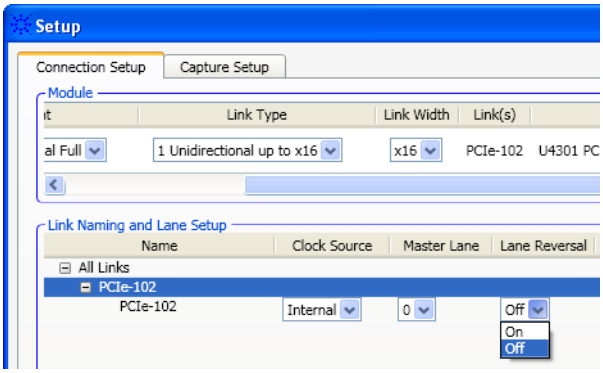


- **Internal** – selects an internal clock source. You should select Internal if the data rate is in the range of 2.5 Gbps or 5 Gbps +/-50 ppm. Note that there is no input clock in this mode.
- **External 1/2/3/4** – selects an external clock source. You should select External if the device under test uses SSC or the data rate is in the range of 2.5 Gbps +/-300 ppm (+0% / -0.5% if using SSC). The clock rate for external mode should be between 100 MHz +/-300 ppm (+0% / -0.5% if using SSC).

7 Select the master lane. You can select any lane as the master lane from the lanes displayed in the Master Lane listbox. The lanes are displayed as per the selected link width. The lane that you select as the master lane is considered the lane for capturing the ordered sets.



8 Specify whether lane reversal is on or off.

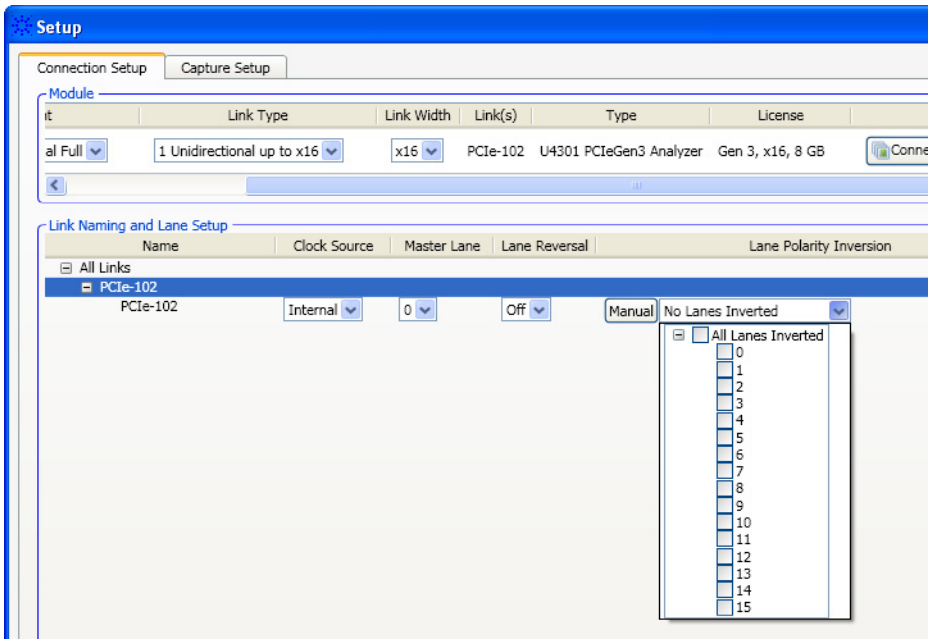


9 Specify any lane polarity inversion:

a Click **Auto** or **Manual** to toggle between the types of polarity inversion specification.

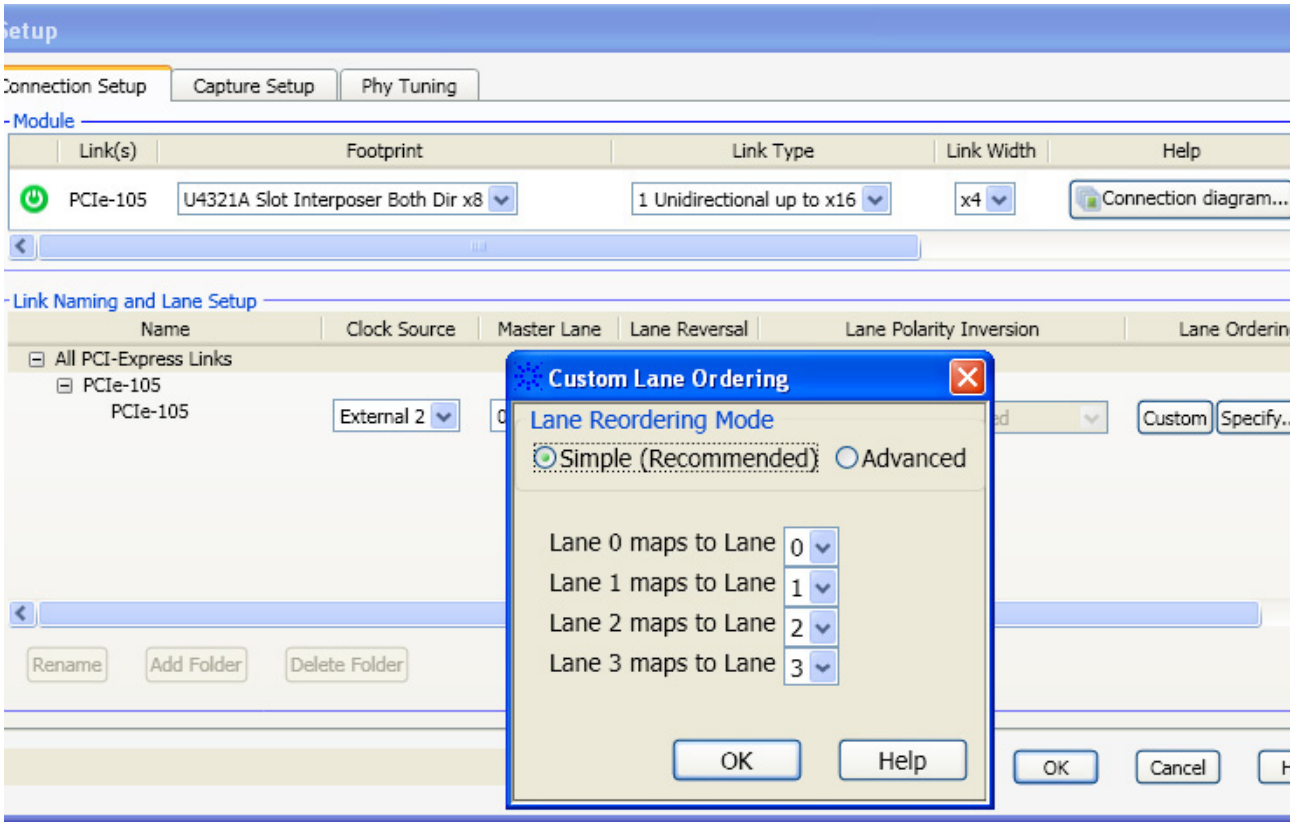
When Auto is selected, the polarity of the lanes is set automatically during the initial link training.

b When manual selection is chosen, select the lanes that are inverted.



10 The **Lane Ordering** option lets you perform the ordering of the physical lanes of the link with the logical lanes. You can either retain the **Default** lane ordering which means Lane 0 of the link maps to logical Lane 0 and so on. If you want to map Lane 0 of the link to some other Lane, then select **Custom** option from Lane Ordering and click **Specify** to display the **Custom Lane Ordering** dialog box. In this dialog box, select the lane with which you want to map Lane 0. The number of lanes displayed for lane ordering depend on the selected link width. For

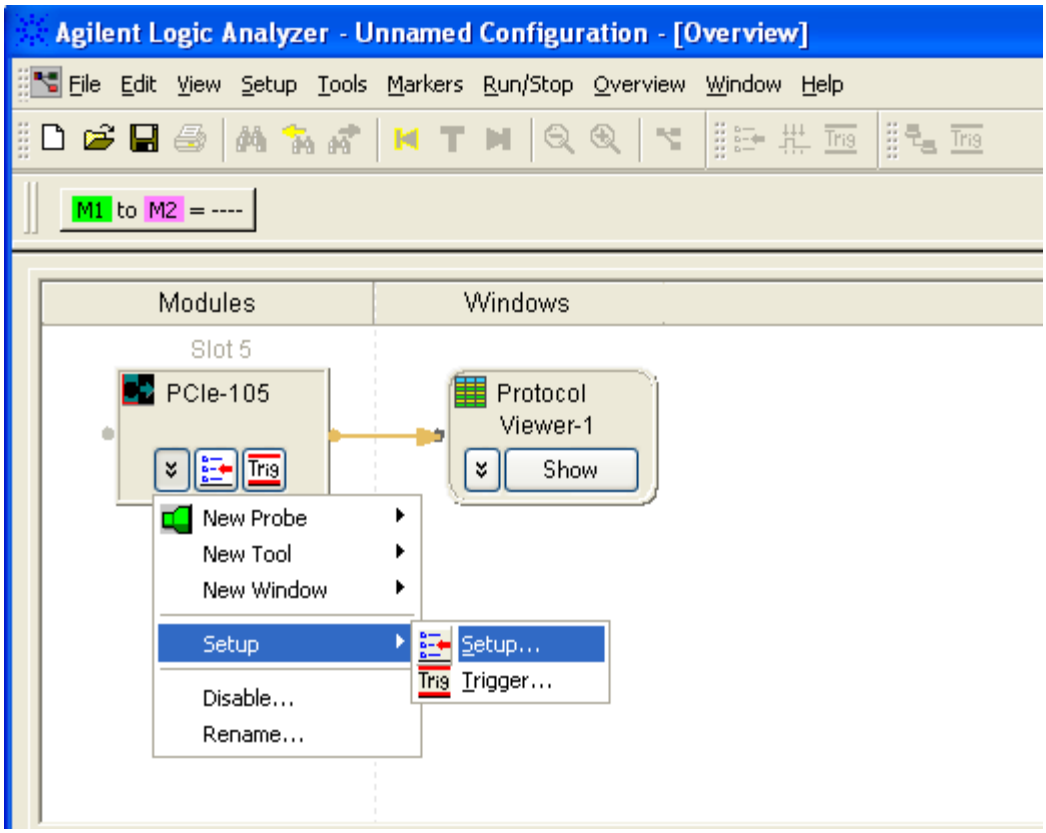
example, if the link width is selected as x4, then the Lane 0, 1, 2, and 3 are available for lane ordering.



4 Setting the Capture Options

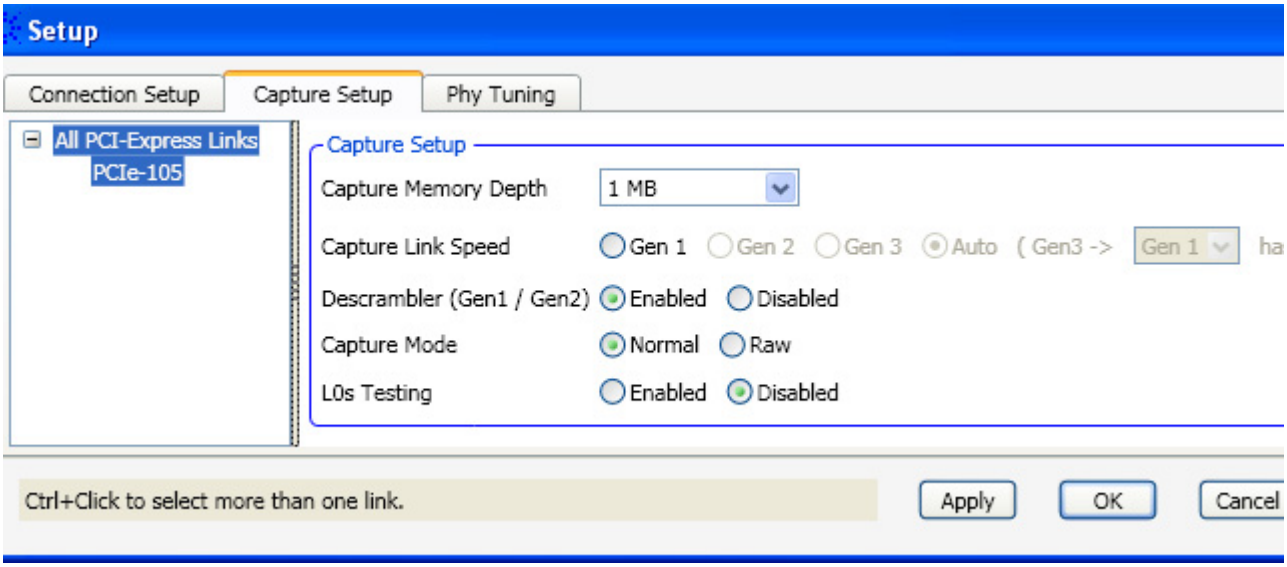
The Capture Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you set basic capture options.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Capture Setup** tab.

3 In the Capture Setup tab, select the appropriate options.



Capture Memory Depth	Lets you select the trace memory depth. Deeper traces capture more activity but take longer to save and process.
Capture Link Speed	Lets you specify the link speed of the data to be captured: • **Gen 1** — select this when capturing data on 2.5 Gbps links. • **Gen 2** — select this when capturing data on 5 Gbps links. • **Gen 3** — select this when capturing data on 8 Gbps links. • **Auto** – select this option when testing link speed switching scenarios. On selecting this option, analyzer automatically detects the link speed change and accordingly starts capturing data based on the changed link speed. The Auto option also has a drop-down listbox displayed with it. From this listbox, you can select either Gen1 or Gen2. If you select **Gen1** from this listbox, then analyzer prioritizes and captures the Gen 1 ordered sets while switching speed from Gen 3. If you select **Gen2** from this listbox, then analyzer prioritizes and captures the Gen 2 ordered sets while switching speed from Gen 3. Based on the selected link speed, the speed LED of the Analyzer pod on which the logical Lane 0 is present will glow. The following color coding is used to interpret the status of the speed LED. • Off - This means that the system is not configured. • Red - This means that the link speed is not detected or not configured. • Yellow - This means that the link speed is 2.5 Gb/s. • Green - This means that the link speed is 5 Gb/s. • Blue - This means that the link speed is 8 Gb/s. If you selected a fixed speed (Gen1, Gen2, or Gen3), then the speed LED will glow according to the selected speed. If you selected the Auto speed option, then the speed LED will glow according to the detected speed.

Descrambler (Gen1 / Gen2)	Tells the analyzer whether the descrambler algorithm is necessary: • **Enabled** — activates the descrambler algorithm. This algorithm generates the descrambled packet stream from an incoming scrambled packet stream. • **Disabled** — deactivates the descrambler algorithm. Select this option when the DUT is transmitting the non-scrambled data. Garbage data is displayed if this is set incorrectly.
Capture Mode	Lets you choose between two capture modes: • **Normal** — captures data only when all the configured lanes are out of the Loss of Sync (LOS) condition, that is, each lane has valid data. In this mode, channel bonding occurs when the analyzer encounters the first SKIP ordered set after exiting from the L0s/L1/L2/recover.speed condition. • **Raw** — captures data by each lane. This means, if only one lane is out of the LOS condition, its data is captured in the trace. In this mode, channel bonding may not exist at all. The Raw mode gives you data visibility even when there are significant PHY layer issues.

L0s Testing	Lets you select whether or not the U4301A module will capture packets in the L0s state.
	• **Enabled** - When you enable the **L0s Testing** option, the U4301A module captures packets in the L0s state and the power management testing capabilities are enabled and enhanced in terms of :
	  • improvement in locking time
	  • faster data capture while coming out of the electrical idle
	• **Disabled** - When you disable the **L0s Testing** option, the power management testing capabilities are available but not enhanced.

NOTE

When testing L0s/L1, ensure that you:

- set manual lane polarity.

- select a fixed capture link speed instead of the Auto speed.

5
Tuning the Analyzer for a Specific DUT

PCIe Gen3 Tuning Overview

What is Tuning

Tuning is the process of adjusting Agilent's probing system to remove the effects of different driving silicon, termination silicon (or other termination schemes), imperfect transmission paths, and the fact that the probes may not be in the "ideal" location for receiving a high-speed signal (that is, at the end of the transmission path).

Furthermore, a PCIe Gen3 system will negotiate its own TX Linear Equalization, and you would like to have the largest eye possible. Tuning does not affect either the transmitter or the receiver; it is used only to increase the eye as seen by the U4301 Analyzer module. This process involves getting the system/device-under-test to a stable PCIe Gen3 transmission state which the analyzer then optimizes its own equalizations settings for.

How Tuning Works

For tuning, you run a tuning algorithm with specific parameters to create a physical layer tuning (.ptu) file. This file contains the information necessary to adjust the probing system for a specific device-under-test (DUT). At the 8 Gbps speed, you then need to load this .ptu file into the U4301 Analyzer module's software to have the best possible eye at the Analyzer. If you want to verify that you have the correct .ptu file, there is a verification program that you can run to analyze the eye quality without re-running the tuning algorithm.

For this release of the Agilent PCIe Gen3 software, you can create or verify a .ptu file for tuning using the command line executables provided by Agilent.

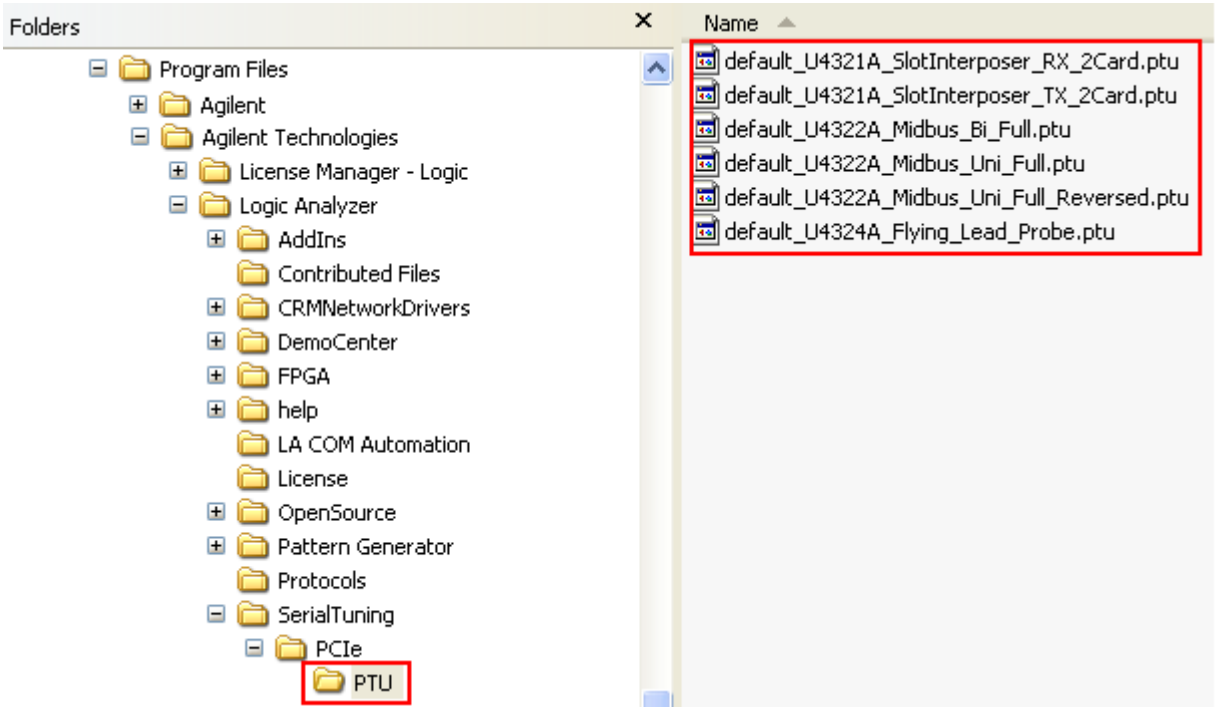
When to Perform Tuning

You should only perform tuning when all of the following conditions are met:

- Poor trace quality which may include red packets, triggers on “Loss of Sync” or “Channel Bonding”.
- No Recovery cycles (that is, cannot Trigger on “Any TS”) on the target.
- When no existing .ptu files are able to provide robust tracing.

Default and User Defined .ptu Files

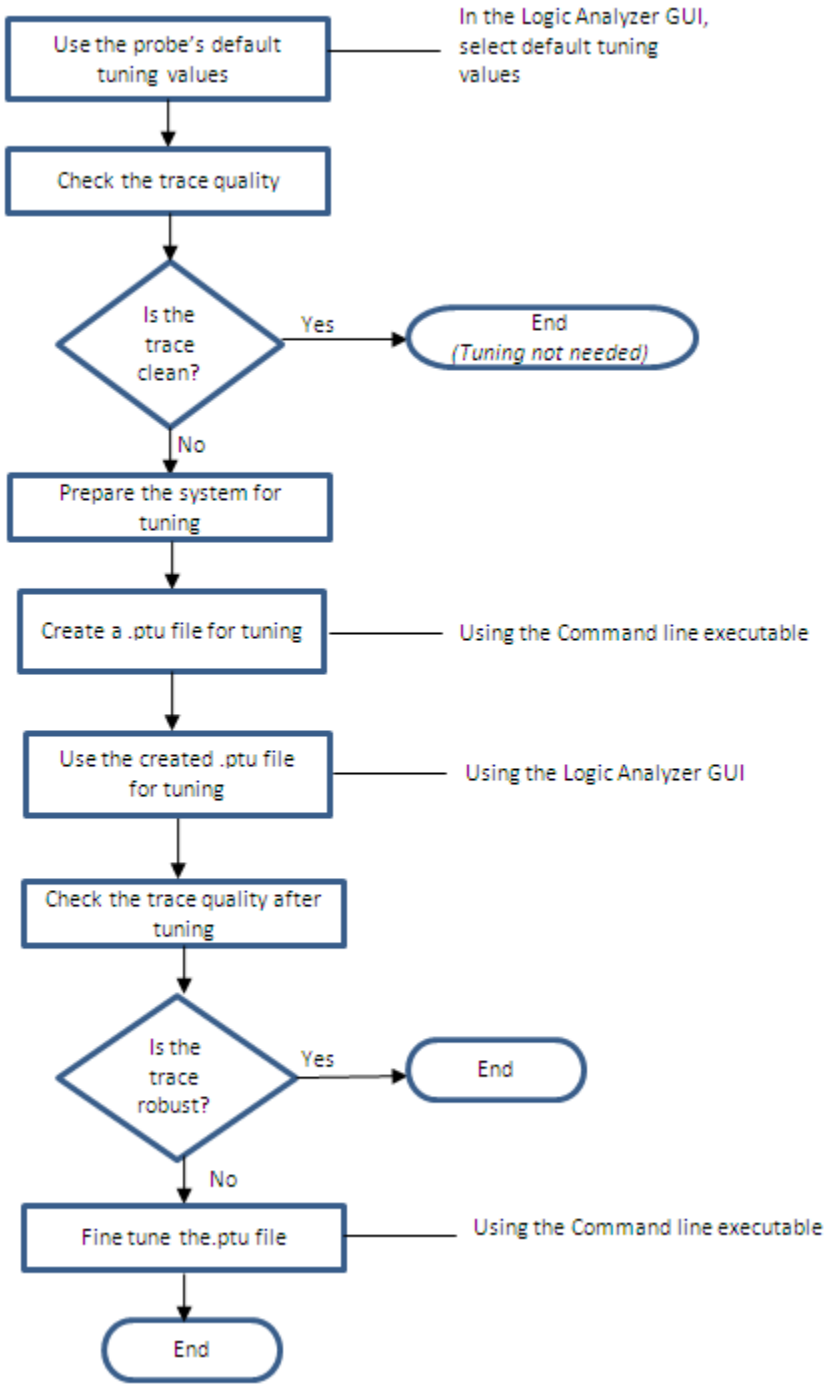
A set of default tuning (.ptu) files are provided with the Agilent Logic Analyzer software. These tuning files contain the probe defaults to compensate for the signal impairments associated with the probe. These files are named on the basis of the probe type for which these are created. Based on the probe type you are using, one of these files is used and if the trace quality is clean, you do not need to tune further by creating your own .ptu file. These default .ptu files work fine and support robust tracing in situations where the targets have margin. The following screen displays the location of these default ptu files.



However, if the default .ptu file does not serve the purpose and you find the trace quality to be poor, you can create your own .ptu file with your specific parameters and use it in the Logic Analyzer GUI to perform tuning. You can create a .ptu file using the command line executable provided by Agilent.

Tuning - Broad steps

The following picture illustrates the broad steps involved in the tuning flow.



All these steps are described in detail in the topics that follow.

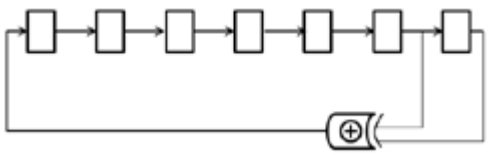
Tuning Methods

While creating the .ptu file using the command line executable, you need to specify the tuning method to be used.

The following tuning methods are currently supported.

- **Logical Idle** - This method is BER based and aims at checking and minimizing a BER only on the Logical Idle periods. No packet transfer is allowed other than periodic Update Flow Control DLLPs. When using the LIDL tuning, the optional command line parameters such as clocking, inversions, update flow control parameters become relevant. This method is suitable for an initial tuning run as well as for fine tuning previous tuning results.
- **AnalogTune** - This method minimizes the deviations of the observed Vertical Eye characteristics versus the desired Vertical Eye characteristics. The Quality of Results of this tuning method are lesser compared to the BER based tuning methods simply because this method optimizes a surrogate metric for BER. However, from the DUT participation perspective, this method only requires the DUT to stay out of Electrical Idle at 8Gbps. The actual traffic on the bus is irrelevant. When using AnalogTune, the optional command line parameters such as clocking, inversions, and update flow control become irrelevant. To perform AnalogTune, use the `--analog` command line option while creating the .ptu file. This method is suitable for an initial tuning run.
- **PRBS23** - This method is BER based and aims at checking and minimizing a BER on every transmitted bit. You can achieve the highest Quality of Results with this method. However, from the DUT participation perspective, this method requires the DUT to transmit PRBS23. When using the PRBS23 method, the optional command line parameters such as clocking and inversions become relevant but the update flow control parameters are irrelevant. To perform PRBS tuning, use the `--prbs` command line option while creating the .ptu file. This method is suitable for an initial tuning run.

  This method assumes that the PRBS polynomial matches the JBERT's PRBS23 $2^{\wedge N-1}$ polynomial: $D^7 + D^6 + 1 = 0$

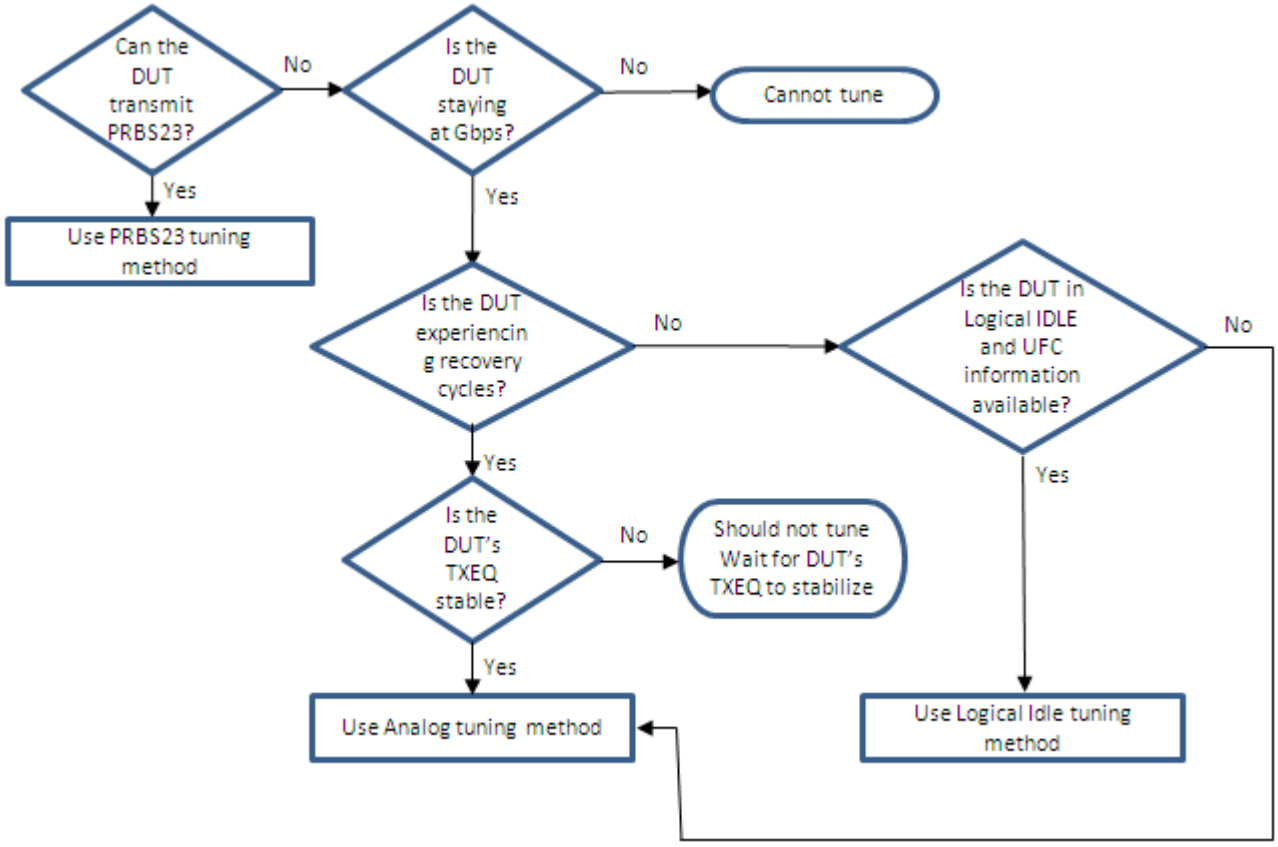


- **SyncHeaders** - This method is BER based and aims at checking and minimizing a BER on only the Block Sync headers. This method requires the DUT to transmit Block Sync headers. When using the SyncHeaders method, the optional command line parameter such as clocking is relevant but the inversions and update flow control parameters are irrelevant. To perform SyncHeaders tuning, use the `--syncheaders` command line option while creating the .ptu file. This method is suitable only for fine tuning and not for an initial tuning run.

To know about how to use these tuning methods, refer to "PCIe Gen3 Tuning Executable and its Usage" on page 37.

Selecting an appropriate tuning method

You can use the following flowchart to decide which tuning method should be used.



Preparing the Analyzer and DUT for Tuning

Perform these steps to prepare the system for tuning:

1 Connect the U4301 Analyzer module to the DUT. Refer to the *PCI Express Gen3 Hardware and Probing Guide* to know how to connect Analyzer to the DUT based on your specific probing situation.

   Take a note of which probing system you have; you will need to specify this as a required information while running the tuning program:

   The following Agilent probing options are supported for use with the Analyzer module.

   - U4321A solid slot interposer.

     Note that there are four connections on this interposer; the upper two are for the "To Upstream" path (assuming that the card plugged into the top connector of the interposer is the downstream side). The lower two connectors are for the "to Downstream" direction.

   - U4322A soft touch midbus 3.0 probe.

     Note that there are several supported footprints that define what lanes are at specific physical connections.

   - U4324A PCIe Gen3 flying lead probe.

     Each of these probes provides support for probing one to four channels of a PCIe link making it a total of 16 channels probing support for a set of four probes.

2 If the Resource Bus connector is connecting two Analyzer modules together (the connector at the left of the modules), remove the Resource Bus Connector and do the tuning of one module at a time.

   After you have tuned, you can reconnect the Resource Bus Connector without affecting the tuning.

3 Your system must enter L0 at Gen3 speed (8 Gbps).

4 For LIDL-based tuning, set up your system so that it is only transmitting the following at 8Gbps:

   a Mostly Logical Idle packets (scrambled zeros).

   b Skip Ordered Sets (optional for the tuning to work, but probably necessary for your system).

   c Update Flow Control DLLPs (again, optional for the tuning process, but part of the PCIe Gen3 specification even when the link is idle).

5 For PRBS tuning, the DUT should be able to transmit PRBS23.

6 For Analog tuning, the DUT must stay out of Electrical Idle at 8Gbps and its TXEQ should have stabilized before tuning. If the DUT is

experiencing Recovery cycles, it is likely that it will change its TXEQ to achieve stability.

7 Gather the following information about your system:

   a The number of lanes in use (1, 2, 4, 8, or 16).

   b Which lanes (if any) are inverted by the transmitter.

Creating a Physical Layer Tuning File

After you have prepared your system for tuning, you can create a physical layer tuning (.ptu) file. This file stores the information about the test setup (lane inversions, number of lanes, etc) and the tuning parameters that were discovered during tuning. You use this file in the PCIe Analyzer setup in the Logic Analyzer GUI to tune the system.

You use the command line executable *PCIeGen3PhyTuning.exe* provided by Agilent to create a physical layer tuning file.

PCIe Gen3 Tuning Executable and its Usage

The following is the usage and a brief description of the required and optional command line options of the PCIe Gen3 tuning executable - ***PCIeGen3PhyTuning.exe***.

Usage

```
PCIeGen3PhyTuning.exe <Required command line options> <Optional
command line options> <PTU file> <PCIe-NNN>
```

Required Command Line Options

Command Line option	Value	Description
--lanewidth	Integer (1, 2, 4, 8, or 16)	The number of lanes that need to be tuned. You can select from 1, 2, 4, 8, or 16 lanes. `Example --lanewidth 4`

Command Line option	Value	Description
--probetype	Possible values: • U4321A_To_Upstream • U4321A_To_Downstream • U4321A_To_Upstream_BidirX8 • U4321A_To_Downstream_BidirX8 • U4322A_Unidirectional_Full • U4322A_Unidirectional_Full_Reversed • U4322A_Bidirectional_Full • U4324A_Flying_Lead • U4324A_Flying_Lead_Upstream_1Card_Bidir_Swizzled • U4324A_Flying_Lead_Downstream_1Card_Bidir_Swizzled	The type of probe and the configuration in which you are using the probe between the U4301 Analyzer module and DUT. You can specify: • **U4321A_To_Upstream** - Specify this probe type if you are using the top two connectors on the U4321A Solid Slot Interposer card to probe the data in the "To upstream" path. • **U4321A_To_Downstream** - Specify this probe type if you are using the bottom two connectors on the U4321A Solid Slot Interposer card to probe the data in the "To downstream" path. • **U4321A_To_Upstream_BidirX8** - Specify this probe type if you are using a U4321A Solid Slot Interposer card in a bidirectional configuration and want to tune the lanes associated with the "To upstream" path. In a bidirectional setup, you tune one direction at a time. • **U4321A_To_Downstream_BidirX8** - Specify this probe type if you are using a U4321A Solid Slot Interposer card in a bidirectional configuration and want to tune the lanes associated with the "To downstream" path. In a bidirectional setup, you tune one direction at a time. • **U4322A_Unidirectional_Full** - Specify this probe type if you are using the U4322A Soft Touch Midbus probe for probing all the 16 lanes in the same direction. • **U4322A_Unidirectional_Full_Reversed** - Specify this probe type if you are using the U4322A Soft Touch Midbus probe for probing all the 16 lanes in the same direction. Reversed refers to optional lane reversal which is supported for upstream ports. • **U4322A_Bidirectional_Full** - Specify this probe type if you are using the U4322A Soft Touch Midbus probe for probing eight lanes in one direction and the remaining eight lanes in the other direction. • **U4324A_Flying_Lead** - Specify this probe type if you are using the U4324A Flying Lead probe for probing 1 - 16 lanes in the same direction. • **U4324A_Flying_Lead_Upstream_1Card_Bidir_Swizzled** - Specify this probe type if you are using a U4324A Flying Lead probe in a bidirectional configuration and want to tune the lanes associated with the "To upstream" path. In a bidirectional setup, you tune one direction at a time. • **U4324A_Flying_Lead_Downstream_1Card_Bidir_Swizzled** - Specify this probe type if you are using a U4324A Flying Lead probe in a bidirectional configuration and want to tune the lanes associated with the "To Downstream" path. In a bidirectional setup, you tune one direction at a time.

Command Line option	Value	Description
--inversions	upto 16 bits	A set of 1s and 0s defining which lanes are inverted on your system as seen by the analysis connector. In the value that you specify for the `--inversions` option, "1" means an inverted lane and "0" means an un-inverted lane and Lane 0 is always the last digit in the inversions value. If Lane Reversal is enabled, then provide a value for the `--inversions` option using the pre-reversal lane definition. *Example* - If you specify the following inversions value for a eight-lane setup, then it indicates that lanes 0,1,and 4 are inverted in this setup. `--inversions 00010011` ***Note***: The `--inversions` command line option is irrelevant if you are performing the Analog tuning (using the `--analog` command line option). For inversion-sensitive tuning methods such as Logical Idle and PRBS23, valid inversion values are required.

Optional Command Line Options

Command Line option	Value	Description
--analog	Not applicable	Use this option to specify that the AnalogTune method should be used for tuning. This option requires the DUT to stay out of Electrical IDLE at 8 Gbps. If you use this command line option, then the `--ufctime`, `--ufcburstlength`, *--extclk*, and `--inversions` command line options do not have any significance.
--prbs	Not applicable	Use this option to specify that the PRBS23 method should be used for tuning. This option requires the DUT to transmit PRBS23. If you use this command line option, then the `--extclk` and `--inversions` command line options are relevant but `--ufctime` and `--ufcburstlength` do not have any significance.
--ufctime	Integer (microseconds)	The minimum time between Update Flow Control DLLP bursts, in microseconds.. See: • "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in LIDL Tuning" on page 44 • "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 43

Command Line option	Value	Description
--ufcburstlength	Integer (between 1 and 15) The default is 3.	The number of back-to-back Update Flow Control DLLPs in a burst. See: • "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in LIDL Tuning" on page 44 • "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 43
--extclk	1 to 4	A number representing the Analyzer module's Pod that the external reference clock is probed on. If you are using the U4321A probe, then this choice must be Pod 2.
--fine	Not applicable	This option fine tunes the results of a previous tuning. It starts with the results of a previously created .ptu file and refines and stores the results in the .ptu file specified as output. Therefore, when you use the --fine option, you must load a previously created .ptu file using the `--loadptu` option. This fine tuning can take quite a bit of time. Refer to "Fine Tuning a .ptu File" on page 50 to know more about fine tuning.
--loadptu	<name and location of the .ptu file>	Use this option when you want to load the results of a previously created tuning file. ***Example*** `--loadptu C:\PCIe_tuning_files\DownstreamAnalog.ptu` This option is particularly significant when you are creating a tuning file for a bidirectional setup or when you are fine tuning the results of a previous tuning. You can also use this option to speed up the tuning basing the tuning on a previous run. See "Tuning a Bidirectional Setup" on page 48 and "Fine Tuning a .ptu File" on page 50 to know more about the usage of this option.
--description	<Filename>	A file describing the test environment setup. If you do not specify any file name, then the tuning program prompts you to type the test environment description.

<PTU File>

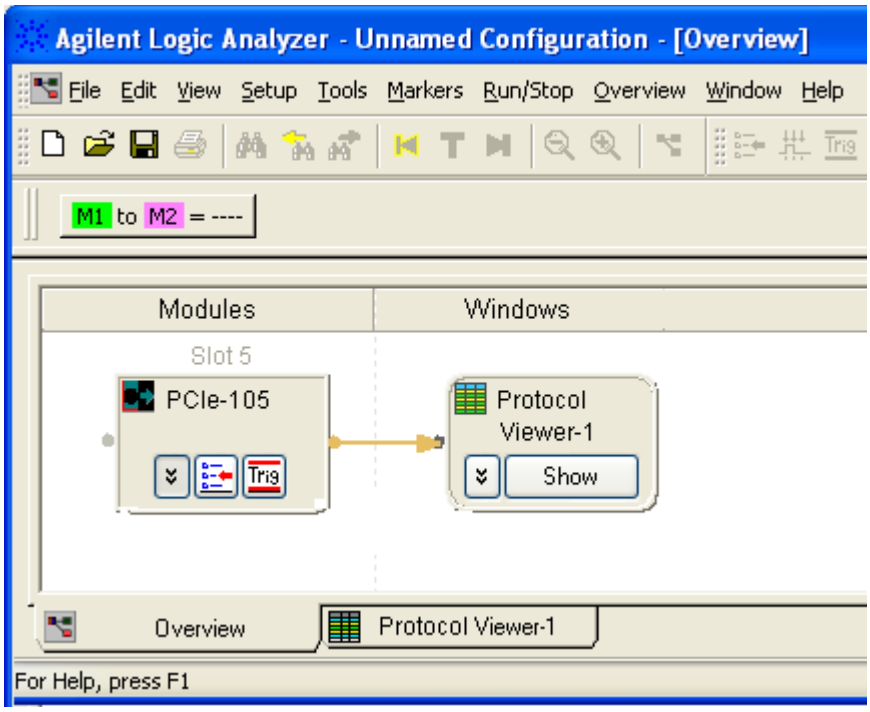
The name and location that you want to provide for the .ptu file. The command to invoke the tuning executable fails if you do not provide the name and location of the tuning file. Ensure that you use explicit file paths while specifying the name and location of the .ptu file.

Example

```
C:\PUT_File\PCIeGen3_Downstream_PTU.ptu
```

<PCIe-NNN>

The name of the U4301 Analyzer module for which you want to create the tuning file. This is the same name with which the U4301 Analyzer module is represented in the Logic Analyzer GUI's Overview tab. For example, PCIe- 101.



The command to invoke the tuning executable fails if you do not provide the name of the Analyzer module.

Tuning Executable Usage - Example

```
PCIeGen3PhyTuning.exe --lanewidth 8 --probetype
U4321A_To_Upstream_BidirX8 --prbs --inversions 0011000 -extclk 2 C:\
PTU_Files\Upstream.ptu PCIe-105
```

In this example, the tuning executable has been invoked to create a tuning file named `Upstream.ptu` at `C:\PTU_Files\` for a bidirectional probing setup configured using the U4321A solid slot interposer card. This command aims at creating a tuning file for tuning only the lanes in the "`To Upstream`" direction.

To create a physical tuning file

Perform these steps on the host PC that is physically connected to the U4301 Analyzer module.

1 Exit the *Agilent Logic Analyzer* application if it is currently active.

2 Start the *Agilent Logic Analyzer* application.

This is done to ensure that all of the default settings in the analyzer software are used.

3 Open a Command prompt.

4 Navigate to the folder where the command line executable (*PCIeGen3PhyTuning.exe*) used for tuning is located. This executable is located at:

<Install location of Logic Analyzer>\SerialTuning\PCIe\Scripts

For example, *C:\Program Files\Agilent Technologies\Logic Analyzer\SerialTuning\PCIe\Scripts*

5 From the navigated location, invoke the tuning executable with the required and optional command line options to start the tuning program.

```
PCIeGen3PhyTuning.exe --lanewidth <lanewidth> --probetype <probetype>
--inversions <inversions> <optional command line flags> <PTU Filename>
PCIe-<NNN>
```

NOTE Ensure that you run the tuning executable from its original location specified in Step 4. If you copy and run it from some other location, it will not be able to find the required DLLs.

The tuning algorithm starts.

The Command Line console displays the results of the tuning algorithm run operation. If the tuning algorithm runs successfully, the .ptu file you specified gets created when the algorithm run completes.

Rectifying the Tuning Parameters

Based on the results of the tuning algorithm displayed in the Command line console, you may want to relook and change some of the tuning parameters specified with the tuning executable. The following are some such situations.

- The tuning output repeatedly displays “ns=-1” for all XVRs for all tests - This may indicate that you need to specify the DUT reference clock path while creating the .ptu file. You do this using the `--extclk` command line option.

- The tuning output repeatedly displays only dots for all XVRs for all tests - This may indicate that you need to specify the DUT reference clock path while creating the .ptu file. You do this using the `--extclk` command line option.
- The tuning output repeatedly displays “ns=-1” for a subset of the XVRs for all tests - This may indicate that you have specified an incorrect value for the `--inversions` command line option while creating the .ptu file. This indication is based on the assumption that you are using an inversions-sensitive tuning method such as Logical Idle or PRBS23.

LEDs display during BER Based Tuning

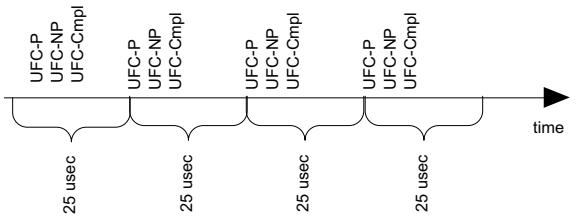
The U4301 Analyzer module has 16 channel LEDs and four status LEDs. The following table lists the interpretation of these LEDs display during BER-based tuning.

Channel LEDs	
Green	Indicates no bit errors on that lane.
Yellow	Indicates loss of sync or “OK”/”ERROR” is toggling quickly. You get “shades of yellow”, usually, when there are frequent bit errors.
Red	Indicates bit error on that lane.
Blinking Red / Off	Indicates input FIFO overflow.
Speed LEDs	
Off	Indicates an Idle state.
Blue	Indicates that the data is being taken.

Understanding "Minimum Time Between UFCs" and "UFC Burst Length"

The PCI Express specification calls on both upstream and downstream components to send out Update Flow Control packets with some maximum time between them. Generally, there are three UFCs per unit time: UFC-Posted, UFC-NonPosted, and UFC-Completions.

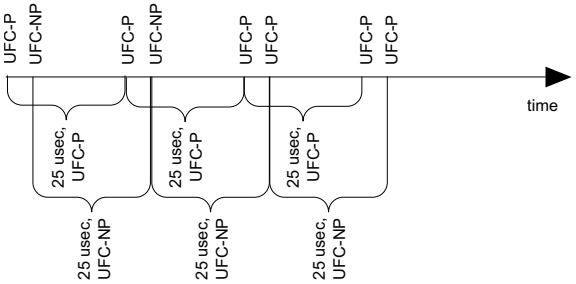
Sometimes the systems send out the UFCs in a "burst". For example, consider a system which, when the link is in Logical Idle, sends out UFCs every 25 micro seconds, and sends them out in a "burst". It might look like this on a graph of UFCs vs time:



For this example, the minimum time between UFCs would be 25 usec, and the UFC Burst Length would be 3.

Another example is where the UFCs come out separated in time, but again have a time of 25 micro seconds between them.

In this example, no UFC-Completions are sent because the endpoint advertised infinite flow control credits. That might look like this:



For this example, the minimum time between UFCs would be 25 usec, and the UFC Burst Length would be 2.

It is probable that the timing is not exact; that is why the input is the "minimum time" between UFCs. So it is normal that for a system that intends to send out UFCs every 25 usec, you might enter 24 usecs.

See Also

- "How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in LIDL Tuning" on page 44

How "Minimum Time Between UFCs" and "UFC Burst Length" is Used in LIDL Tuning

Tuning is done by looking at logical idle states in 8 Gbps mode (Gen3) and creating a Bit Error Rate Test based on the LFSR XOR'ed with 0's.

To get an accurate count, the non-zero data that normally occurs during a stream of logical idles – EDS TLLPs, SKP Ordered Sets, EIEOS, etc. – need to be detected and ignored. To reduce the dependency of tuning on an exactly correct protocol, a minimum number of dependencies on the protocol are used.

Update Flow Control packets are normally sent when a link is in the logical idle state. In order to ignore the "real" update flow control packets, but not demand that they be 100% correct, the tuning algorithm needs to know about how often they are sent.

If a value given the tuning algorithm is too small (that is, the UFCs are actually sent less often than the turning algorithm is told), the only thing that happens is that some errors that are signal integrity errors will be ignored; in this case, taking a trace after the tuning will show what the real time between UFCs are, and another tuning can be done with the correct values.

If the values given to the tuning algorithm is too high (that is, the UFCs are actually sent more often than the tuning algorithm is told), then some UFCs will be counted as signal integrity errors, and the tuning algorithm might take longer to complete and perhaps return suboptimal tuning. Again, in this case, after the tuning is performed a trace will show the correct timing between UFCs, and the next tuning can take that information into account to reduce the time to run and get more accurate results.

If there is no knowledge about the UFCs for a given target, enter small number for the time between UFCs – say 10 usecs – and "3" for the burst count (see "Understanding "Minimum Time Between UFCs" and "UFC Burst Length"" on page 43).

Tuning Time vs Eye Quality at Analyzer

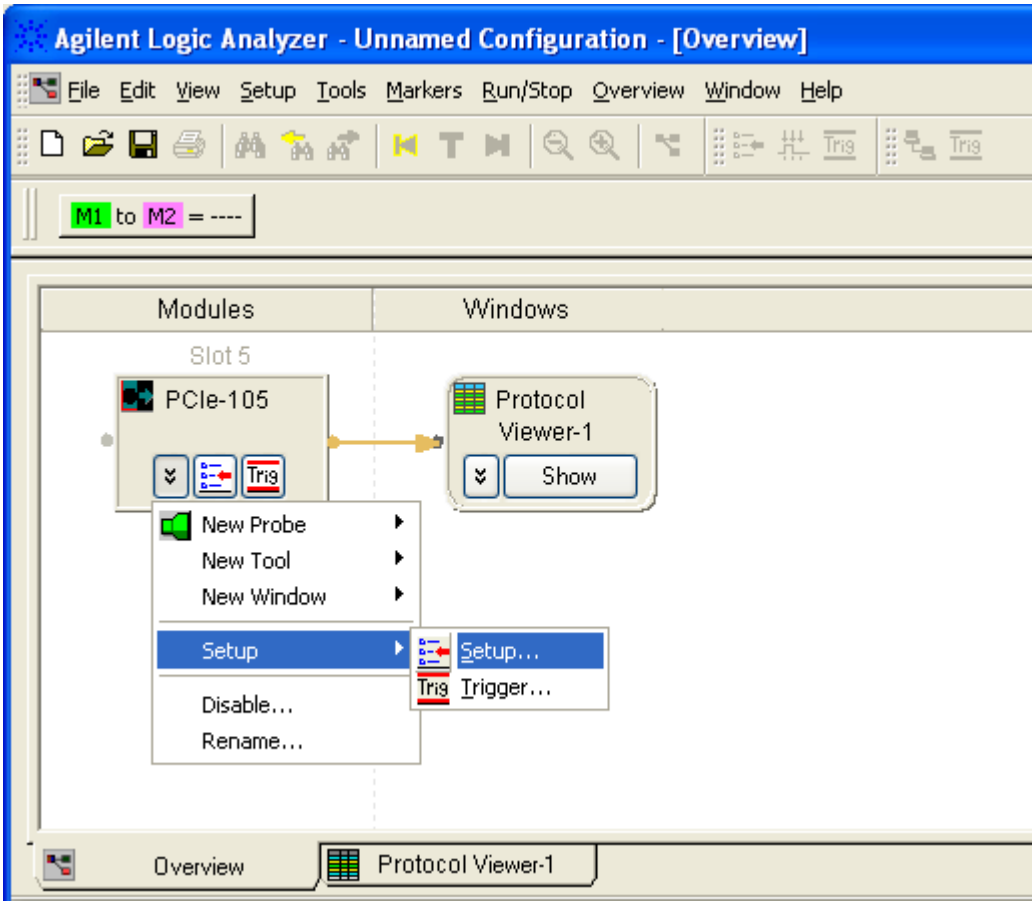
There is a trade-off between how long you want the analyzer to spend tuning its characteristics for a specific setup versus your needs. Depending on your analysis needs, you may choose to spend less time tuning in order to start analysis of your system quicker. Here is one way to think about it:

If you will be taking short traces, and the majority of time the data is being ignored, you can tune for a shorter period of time (and thus, potentially, tolerate a lower quality eye at the analyzer). Think about it in terms of the percentage of data you "care" about versus the percentage of data you don't care about, and the chance that (random) bit errors will occur during the time you are taking data.

Using the Tuning File in the Logic Analyzer GUI

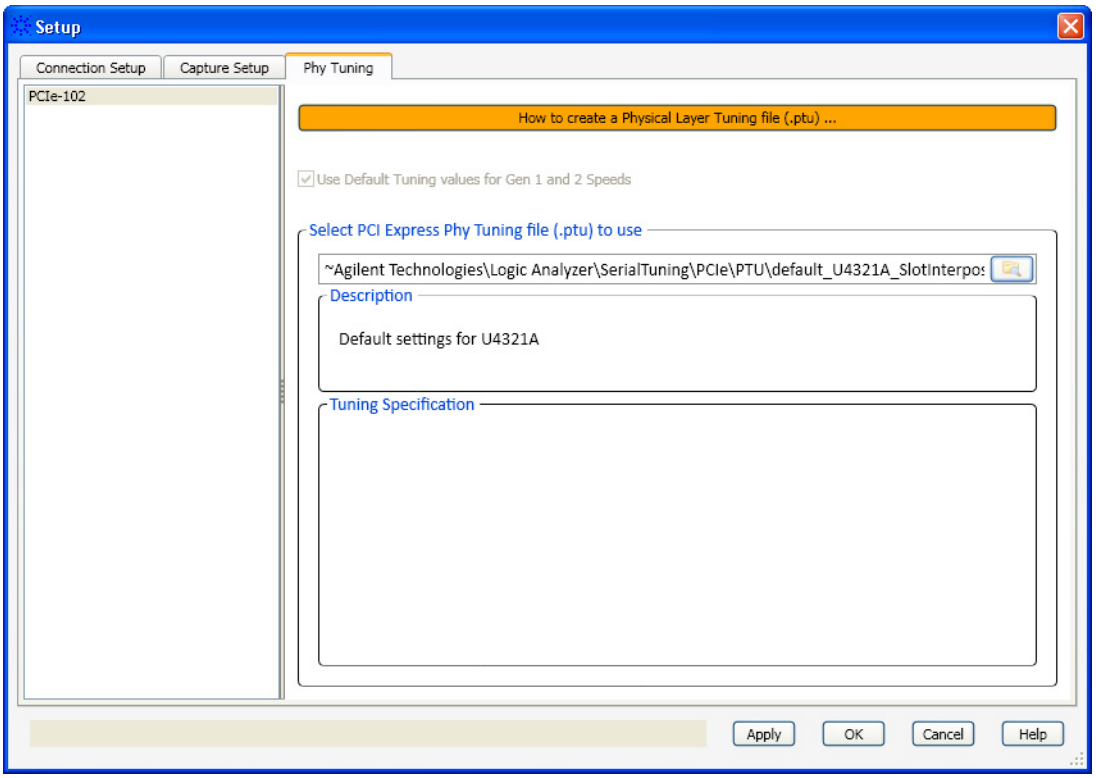
The Phy Tuning tab in the PCIe Gen3 analyzer's Setup dialog lets you select a physical tuning (.ptu) file or the default tuning values for setting up Equalizing Snoop Probes (ESPs) settings.

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Phy Tuning** tab.

3 In the Phy Tuning tab, browse to select the .ptu file that you want to use as the tuning file.



4 Click **Apply** or **OK**.

Tuning a Bidirectional Setup

When tuning a bidirectional configuration, you need to tune one direction at a time.

If you are using the U4301 Analyzer module and probes in a bidirectional configuration, you need to perform the tuning as follows:

1 **Create a physical tuning file for one direction** - In this step, run the tuning command line executable with the probe type reflecting either the upstream or downstream direction of a bidirectional setup.

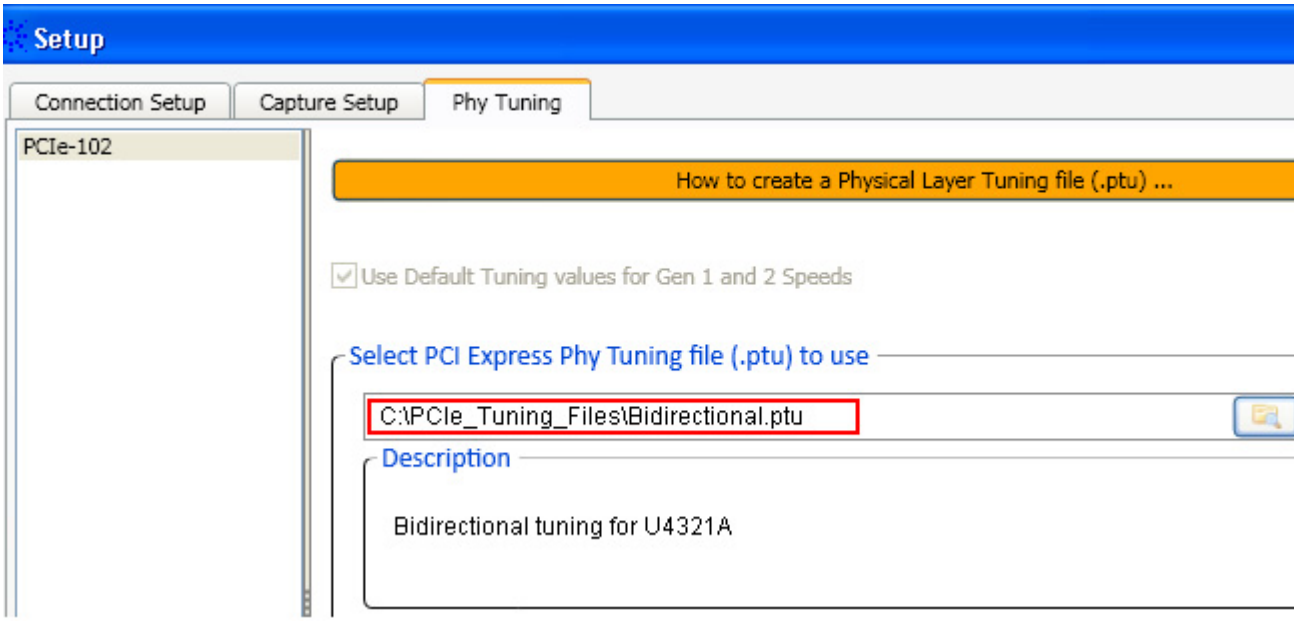
Example - `PCIeGen3PhyTuning.exe --lanewidth 8 --probetype U4321A_To_Downstream_BidirX8 --ufctime 25 --ufcburstlength 3 --inversions 00000000 --extclk 2 c:\PCIe_Tuning_Files\Downstream.ptu PCIe-102`

2 **Tune the other direction** - Run the tuning command line executable with the probe type reflecting the other direction and loading the .ptu file that was the output in Step 1. By loading the .ptu file generated in Step 1, the output .ptu file that you finally get from step 2 has tuning details for both the directions and you do not need to manually merge two different .ptu files.

Example - `PCIeGen3PhyTuning.exe --lanewidth 8 --probetype U4321A_To_Upstream_BidirX8 --ufctime 25 --ufcburstlength 3 --inversions 00000000 --extclk 2 --loadptu C:\PCIe_Tuning_Files\Downstream.ptu C:\PCIe_Tuning_Files\Bidirectional.ptu PCIe-102`

NOTE Both upstream and downstream directions share a common reference clock. Therefore, specify the same value for the `-extclk` command line options while running the tuning executable for upstream and downstream directions.

3 **Use the output .ptu file generated in Step 2 in the Logic Analyzer GUI** - Instead of using the default probe values, use the output file generated for both the directions in the Logic Analyzer GUI.

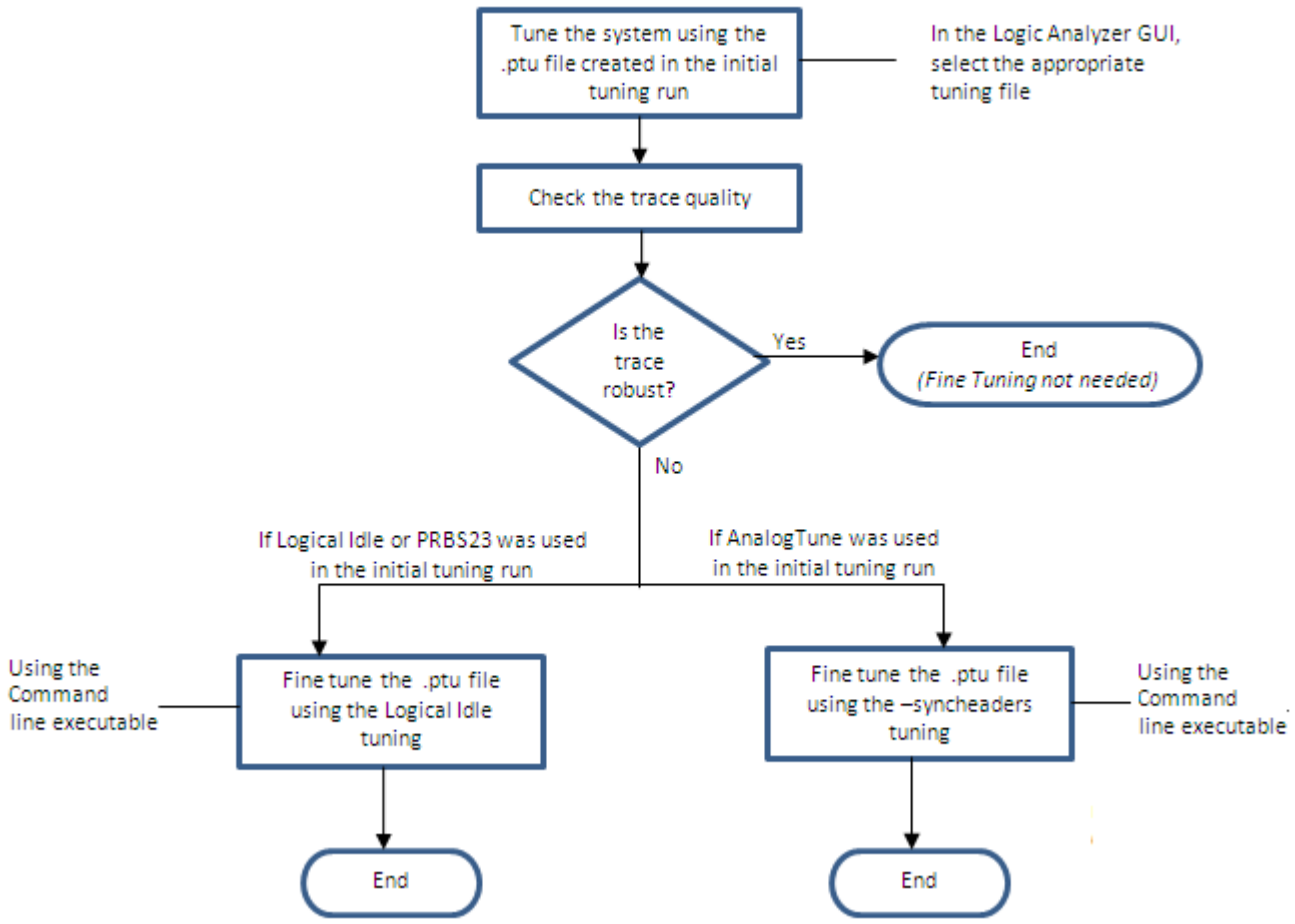

Setup
Connection Setup
Capture Setup
Phy Tuning
PCIe-102
How to create a Physical Layer Tuning file (.ptu) ...
Use Default Tuning values for Gen 1 and 2 Speeds
Select PCI Express Phy Tuning file (.ptu) to use
C:\PCIe_Tuning_Files\Bidirectional.ptu
Description
Bidirectional tuning for U4321A

Fine Tuning a .ptu File

If the .ptu file that you created does not produce robust and clean tracing, then you can fine tune the .ptu file to get the desired results from tuning.

Fine Tuning Flow

The following picture illustrates the fine tuning flow.



To fine tune a .ptu file

1. From the Command prompt, navigate to the location where you have stored the tuning command line executable `PCIeGen3PhyTuning.exe`.
2. Run the tuning executable with the `--fine` and `--loadptu <.ptu file to be tuned>` command line options.

The results of the fine tuning run are stored in the output .ptu file that you specified in the command.

NOTE The AnalogTune method is not supported for fine tuning a .ptu file. This means that you cannot use `--analog` command line option when using the `--fine` option.

Fine tuning - examples

Example 1 - In the following example, the *DownstreamLIDL.ptu* file is loaded for fine tuning using the default Logical Idle tuning method and the output of fine tuning is specified as *DownstreamLIDLFineTuned.ptu*. Notice the usage of the `--loadptu` and `--fine` command line options to accomplish fine tuning.

```
PCIeGen3PhyTuning.exe --lanewidth 8 --probetype
U4321A_To_Downstream --inversions 01001010 --ufctime 3
--ufcburstlength 3 --extclk 2 --loadptu c:\
PCIe_Tuning_Files\DownstreamLIDL.ptu --fine c:\
PCIe_Tuning_Files\DownstreamLIDLFineTuned.ptu PCIe-102
```

Example 2 - In the following example, the *UpstreamAnalog.ptu* file is loaded for fine tuning using the Syncheaders tuning method and the output of fine tuning is specified as *UpstreamSyncheadersFineTuned.ptu*. Notice the usage of the `--loadptu --fine`, and `--syncheaders` command line options to accomplish fine tuning.

```
PCIeGen3PhyTuning.exe --lanewidth 8 --probetype
U4321A_To_Upstream --inversions 01001010 --extclk 2
--loadptu c:\PCIe_Tuning_Files\UpstreamAnalog.ptu --fine
--syncheaders c:\PCIe_Tuning_Files\
UpstreamSyncheadersFineTuned.ptu PCIe-102
```

Verifying a Tuning File

When changes occur to your system (new silicon, new connections, or maybe even after re-seating connectors), you may want to verify that you do not need to re-tune the Analyzer for the new setup. You can check whether or not re-tuning is needed by verifying the existing .ptu file used for tuning.

To verify a tuning file, you need not re-run the complete tuning program. Instead, you run the Verification program by invoking the tuning verification executable, *PCIeGen3PhyVerifyTuning.exe* provided by Agilent.

Before starting the verification procedure, attach the U4301 Analyzer module to your DUT and set up your system so that it is mostly transmitting Logical Idles (see "Preparing the Analyzer and DUT for Tuning" on page 35).

To verify a tuning file

1. Exit the *Agilent Logic Analyzer* application if it is currently active.
2. Start the *Agilent Logic Analyzer* application.

   This is done to ensure that all of the default settings in the analyzer software are used.
3. Open a Command prompt.
4. Navigate to the folder where the command line executable (*PCIeGen3PhyVerifyTuning.exe)* used for tuning verification is located. This executable is located at:

   <Install location of Logic Analyzer>\SerialTuning\PCIe\Scripts

   For example, *C:\Program Files\Agilent Technologies\Logic Analyzer\SerialTuning\PCIe\Scripts*
5. From the navigated location, invoke the tuning verification executable with the command line options to start the verification program.

NOTE Ensure that you run the verification executable from its original location specified in Step 4. If you copy and run it from some other location, it will not be able to find the required DLLs.

The following is the usage of this executable and a description of its command line options.

```
PCIeGen3PhyVerifyTuning.exe --short --verylong --quiet --extclk
<Number> <PTU Filename> PCIe-<NNN>
```

Command Line option	Value	Description
--short	Not applicable	Specifies that the verification test should run for about 3 seconds - about 10^{10} bits.: If you do not specify any command line option for the test length, then the test runs for about 3 minutes - about 10^{12} bits). This is the default.
--verylong	Not applicable	Specifies that the verification test should run for 9 minutes - about $4*10^{12}$ bits: If you do not specify any command line option for the test length, then the test runs for about 3 minutes - about 10^{12} bits). This is the default.
--quiet	Not applicable	If you specify this option, then the verification program prints “All pass” if all tests passed or “Some failed” as soon as a test fails.
--extclk	Integer (1 to 4)	A number representing the Analyzer module’s Pod that the external reference clock is probed on. If you are using the U4321A probe, then this choice must be Pod 2.
<PTU Filename>	Name and location of the .ptu file	The name and location of the .ptu file that you want to verify. The command to invoke the tuning executable fails if you do not provide the name and location of the tuning file. Ensure that you use explicit file paths while specifying the name and location of the .ptu file. ***Example*** `C:\PUT_File\PCIeGen3_Downstream_PTU.ptu`
PCIe-<NNN>	Name of the U4301 Analyzer module	The name of the U4301 Analyzer module for which you want to verify the tuning file. This is the same name with which the U4301 Analyzer module is represented in the Logic Analyzer GUI’s Overview tab. For example, PCIe-101.

The verification program starts and displays the test environment details with which the tuning file was created.

During the test, a seconds-counter will count down. It does not necessarily reach "0" before the number of bits tested have been observed (the counter is for a worst-case number of Skip Ordered Set blocks and Update Flow Control packets).

After the test is finished, a summary of errors is printed, which displays the lanes that have passed or failed.

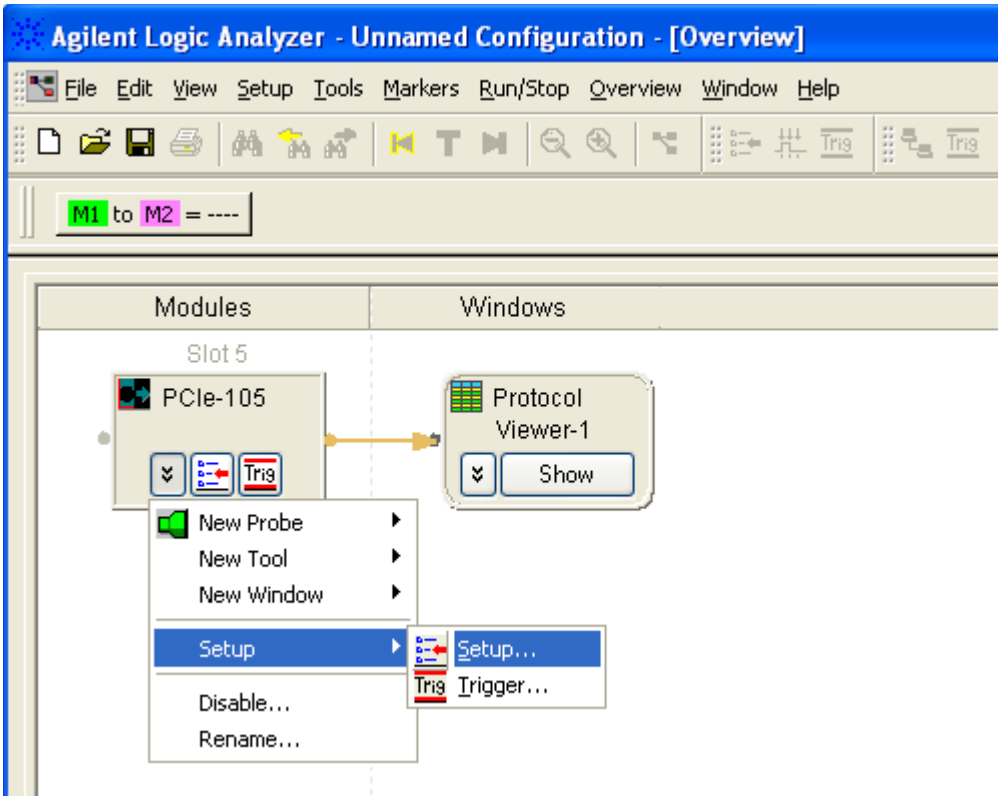
If any lane fails, make sure that Logical Idles are being transmitted on that lane. If they are, you should re-run the tuning algorithm on all lanes. (It does not take any more time to run tuning on all active lanes vs. a single active lane because the tests are all run in parallel.) This will update the .ptu file for all active lanes.

6 Manually Adjusting the Equalizing Snoop Probe (ESP) Settings

The Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog lets you manually adjust the equalizing snoop probe (ESP) settings.

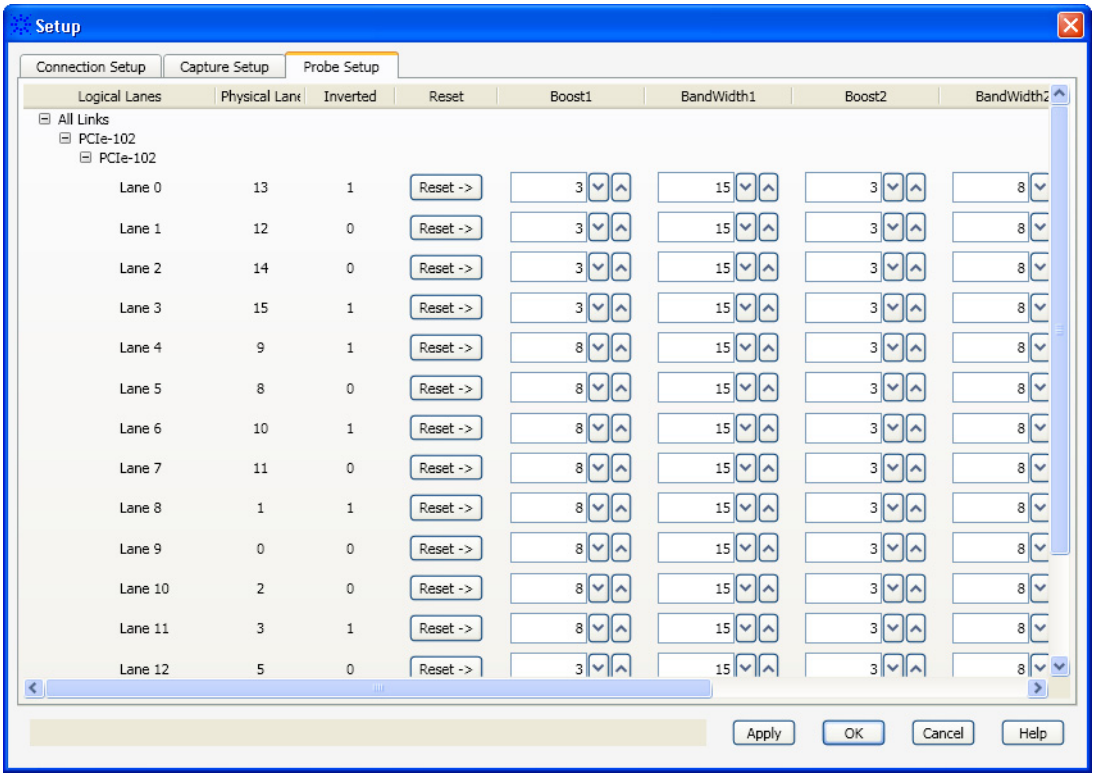
NOTE To enable the Probe Setup tab in the PCIe Gen3 analyzer's Setup dialog, you must check the Enable Advanced Probe Settings (ASP) option in the Options dialog. See "Options Dialog" (in the online help).

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe Gen3 analyzer module's drop-down menu, select **Setup>Setup...**.



2 Click the **Probe Setup** tab.

3 In the Probe Setup tab, select the appropriate options.



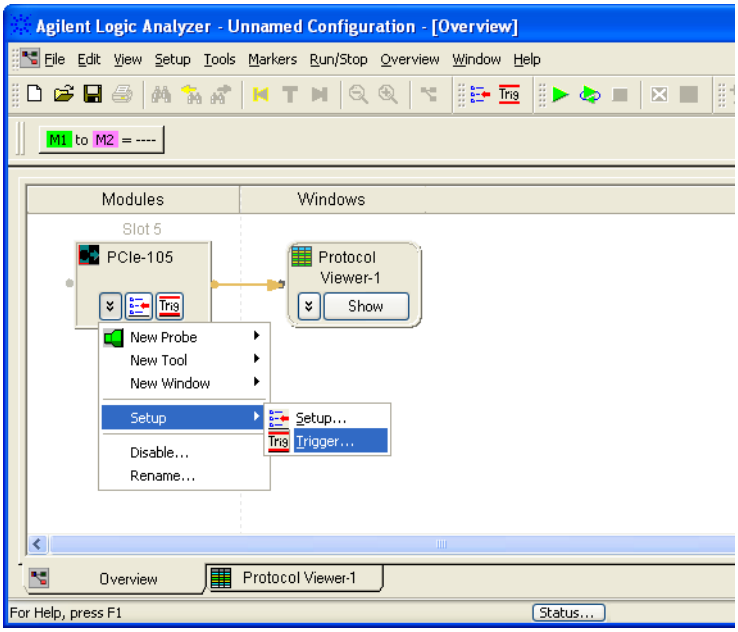
For each lane in the links, you can adjust the boost and bandwith settings. Click **Reset ->** to restore the original settings.

7 Setting Up Triggers

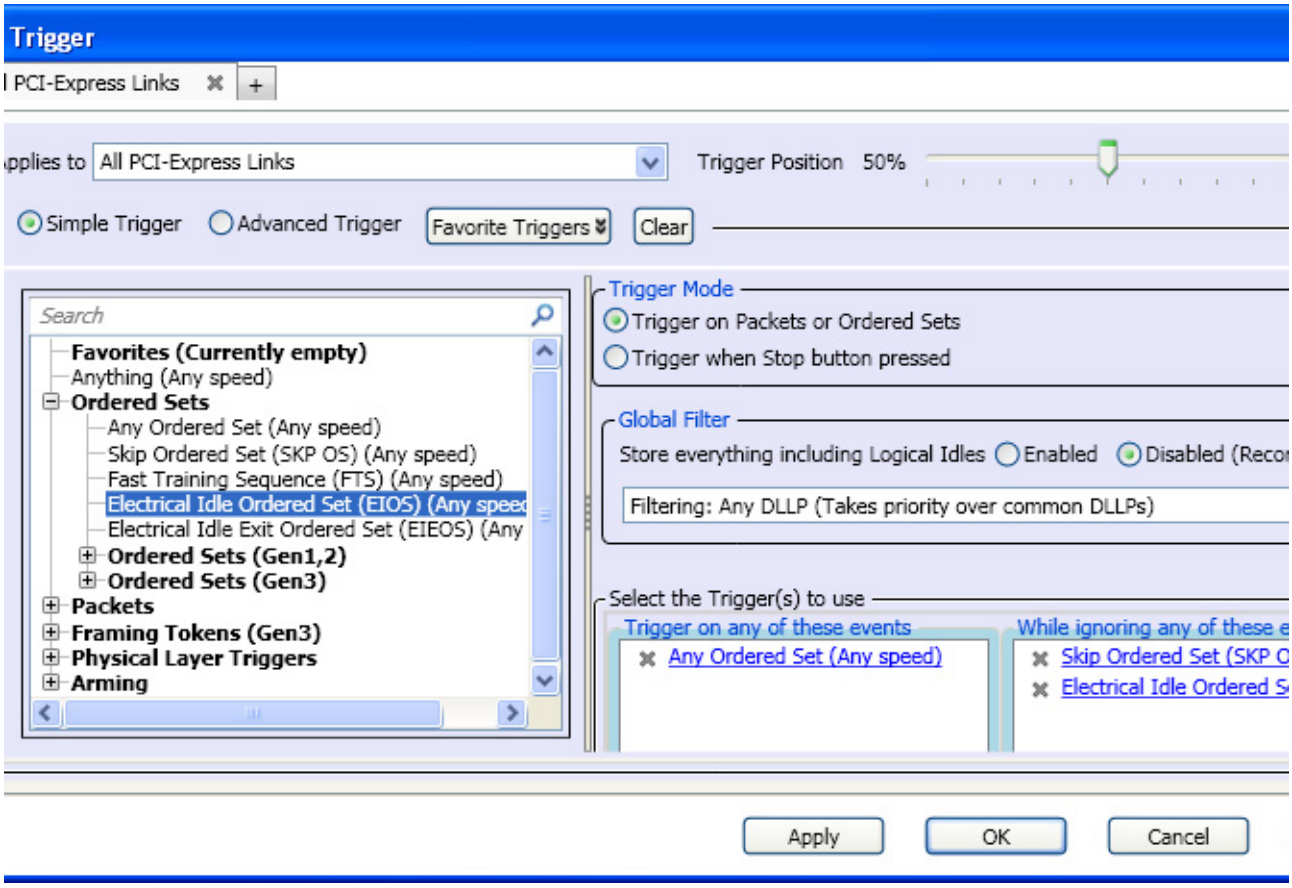
The U4301A PCIe Gen3 analyzer lets you set up triggers (events that specify when to capture a trace) with simple or advanced dialogs.

Setting Up Simple Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Simple Trigger** option.

b Select the **Trigger on Packets or Ordered Sets** Trigger Mode option.

(The **Trigger when Stop button is pressed** Trigger Mode option can be useful, for example, to see the events that lead up to a stop, halt, etc.)

c From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a result, analyzer will keep running and you need to stop it

manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you would like to trigger on from the left-side pane to the **Trigger on any of these events** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed.

To edit events in the trigger box, click the underlined event name.

To remove events from the trigger box, click the "X" to the left of the event name.

d Drag events you'd like to exclude from the trigger to the **While ignoring any of these events** box.

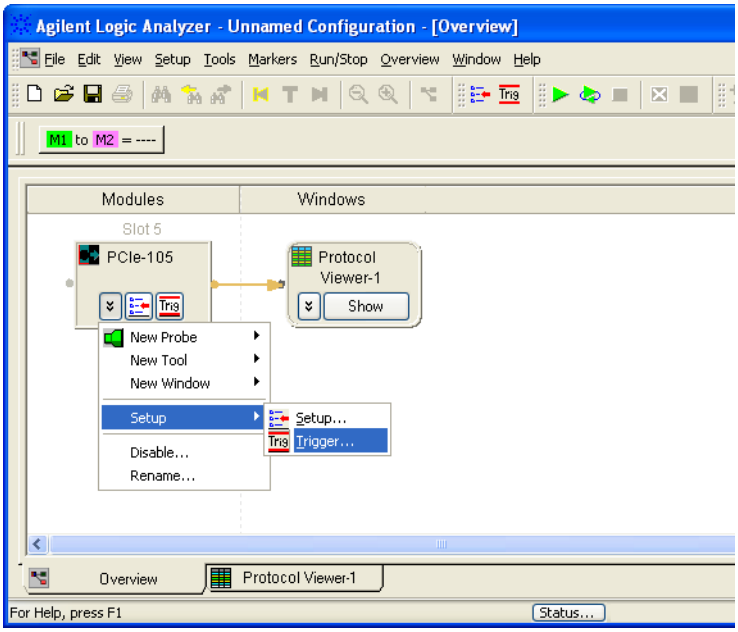
e Click **Apply** or **OK**.

See Also

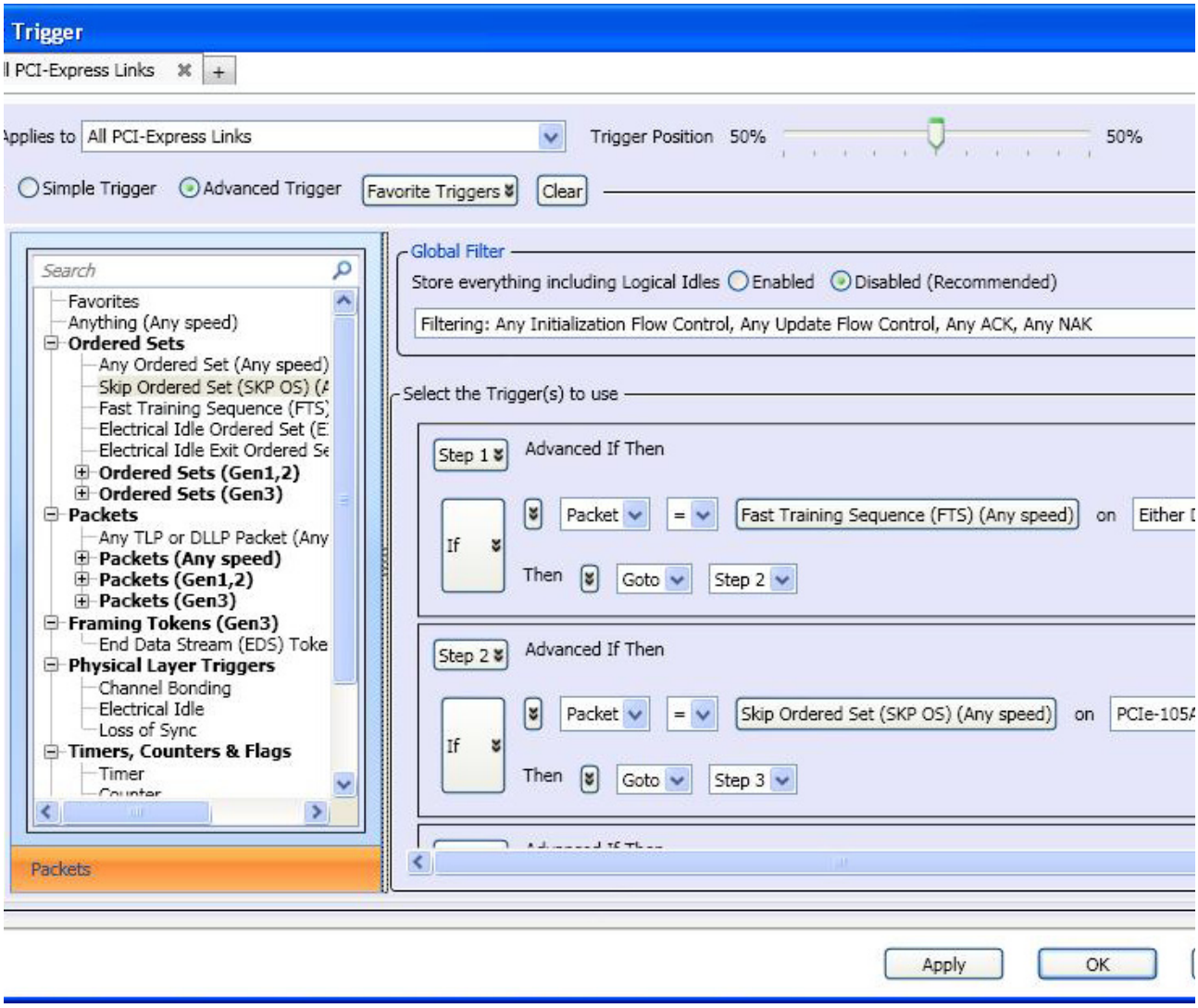
- "To select which links the trigger is for" on page 64
- "To set the trigger position" on page 64
- "To save/recall favorite triggers" on page 65
- "To clear the current trigger" on page 65

Setting Up Advanced Triggers

1 In the *Agilent Logic Analyzer* application's Overview window, from the PCIe analyzer module's drop-down menu, select **Setup>Trigger...**.



2 In the Trigger dialog:



a Select the **Advanced Trigger** option.

b From the **Global Filter** listbox, select the following two options:

i Select whether you want to enable or disable the storage of all types of ordered sets and packets including the logical idles in the capture memory.

ii If you disable the storage of everything including the logical idles, then this drop-down list is activated. From this list, you can select the types of ordered sets and TLP/DLLP packets that you want to filter out from getting stored in analyzer memory. The options selected from this list act as the storage qualifiers. The selected types of ordered sets and packets are acquired but are not qualified to be stored in the analyzer's memory. If you select the **Filter Everything** option from this list, then none of the acquired samples will qualify to be stored in the analyzer memory. As a

result, analyzer will keep running and you need to stop it manually because analyzer keeps acquiring data until the memory depth is full. If you do not select any option from the list, then the filtering is considered Off and all the acquired data is stored in memory when the trigger condition is met.

c Drag events you'd like to trigger on from the left-side pane to sequence steps in the **Select the Trigger(s) to use** box.

The left-side pane contains an event hierarchy that can be expanded or collapsed. (This is the same event hierarchy displayed in the simple trigger dialog.)

To edit events in the trigger box, click the event button.

To remove events from the trigger box, click the sequence step buttons.

d In the **Select the Trigger(s) to use** box, click buttons, make drop-down selections, and enter values in fields to edit the steps in the trigger sequence:

- The **Step** buttons let you insert or delete steps.
- The **If**/**Else if** buttons let you insert or delete "if" clauses.
- The event chevron buttons let you insert, delete, or logically group (or negate) events.
- The direction drop-down listbox is displayed if you configured the U4301A module's connection setup as a bidirectional setup. It lets you select the direction (upstream or downstream) applicable for the trigger sequence. For a unidirectional data capture setup, this listbox is not displayed.
- The action chevron buttons let you insert or delete actions.
- Use the **Comment** fields to document your advanced triggers.

e Click **Apply** or **OK**.

See Also

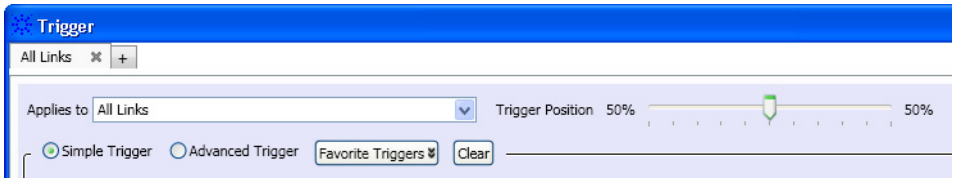
- "To select which links the trigger is for" on page 64
- "To set the trigger position" on page 64
- "To save/recall favorite triggers" on page 65
- "To clear the current trigger" on page 65

Setting General Trigger Options

The top part of the Trigger dialog contains general options that apply to both simple and advanced triggers.

To select which links the trigger is for

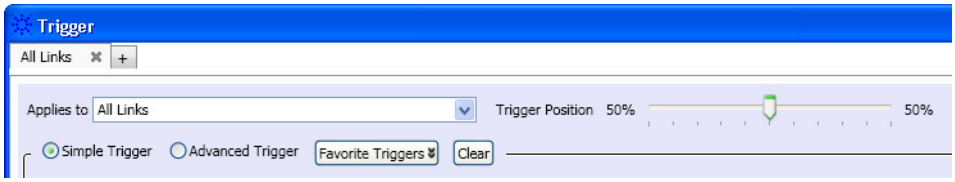
The top of the Trigger dialog has tabs that let you set up separate triggers for different links. You can add tabs for separate triggers and apply them to the links that are set up in the Connection Setup dialog (see Chapter 3, “Specifying the Connection Setup,” starting on page 13).



To set the trigger position

The top of the Trigger dialog has a slider for setting the trigger position within the capture memory.

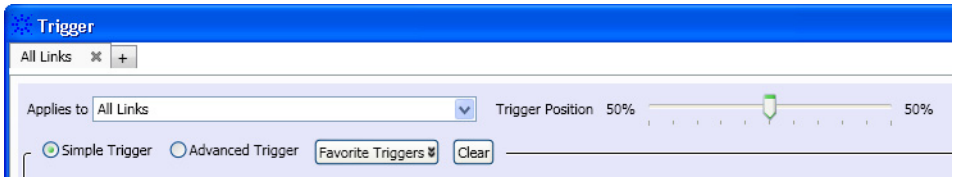
Note that the pre-trigger portion of the capture memory is filled before searching for the trigger.



To save/recall favorite triggers

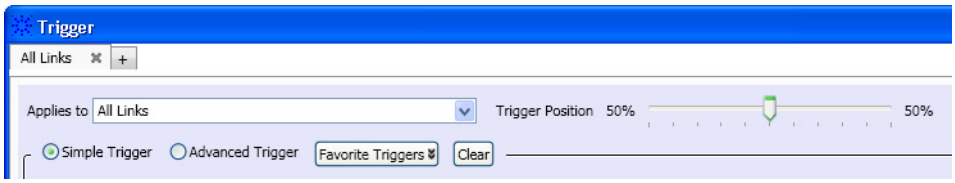
The top of the Trigger dialog has a **Favorite Triggers** drop-down menu for saving trigger setups and recalling previously saved trigger setups.

Do not confuse these "favorite" triggers with the favorites that appear in the left-side pane (which are added using the Event Editor dialog).



To clear the current trigger

The top of the Trigger dialog has a **Clear** button for erasing the current trigger setup and restoring the default trigger setup.

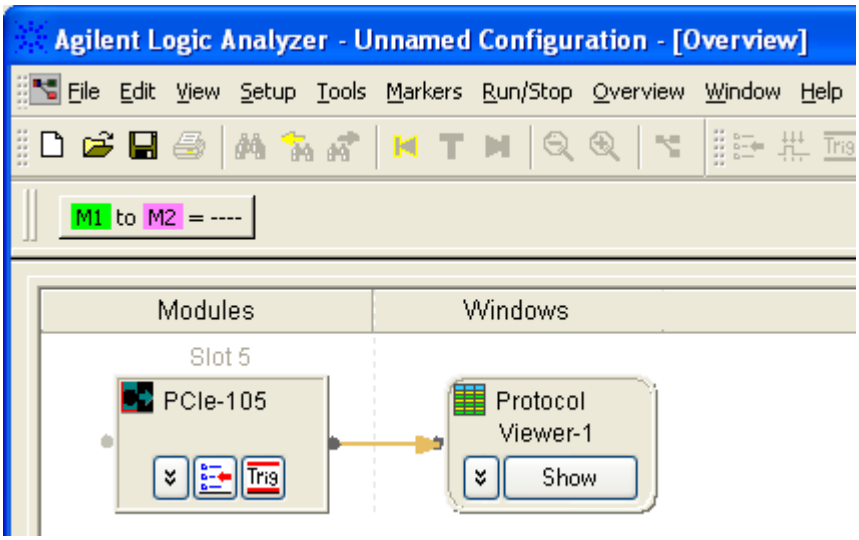


8 Running/Stopping Captures

Running and stopping the U4301A PCIe Gen3 analyzer is just like running and stopping any other analyzer. See "Running/Stopping Measurements" (in the online help).

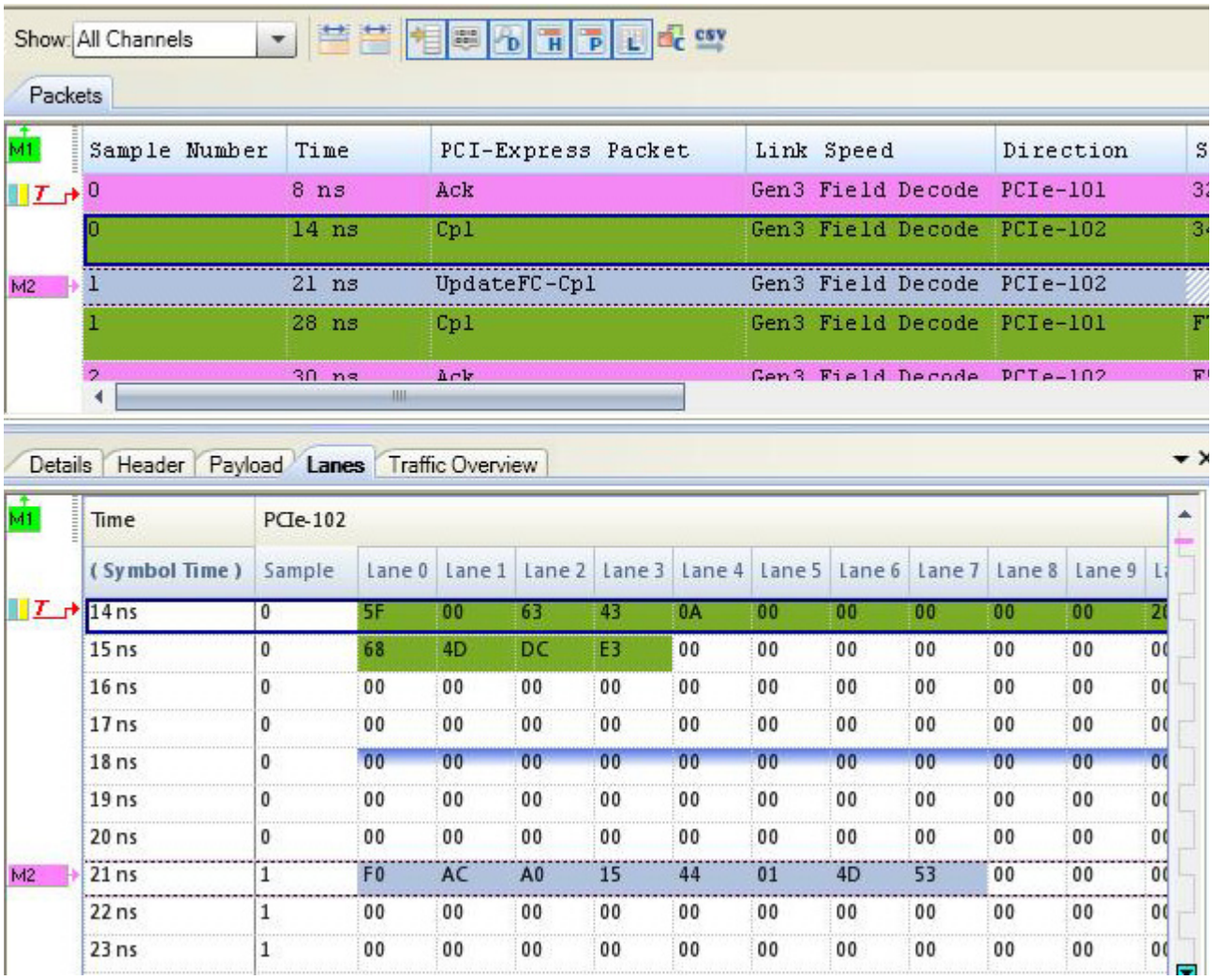
9 Viewing PCIe Gen3 Packets

You can view the data captured by the U4301A PCIe Gen3 analyzer using the Protocol Viewer window. See “Analyzing Packet Data” (in the Agilent Logic Analyzer online help). A Protocol Viewer is automatically added for a U4301A PCIe Gen3 analyzer module in the Logic Analyzer GUI.



The Protocol Viewer window displays the summarized and detailed packet information at the same time within two panes. The upper pane lists the packets. On selecting a packet, the details of that packet are displayed in the lower pane.

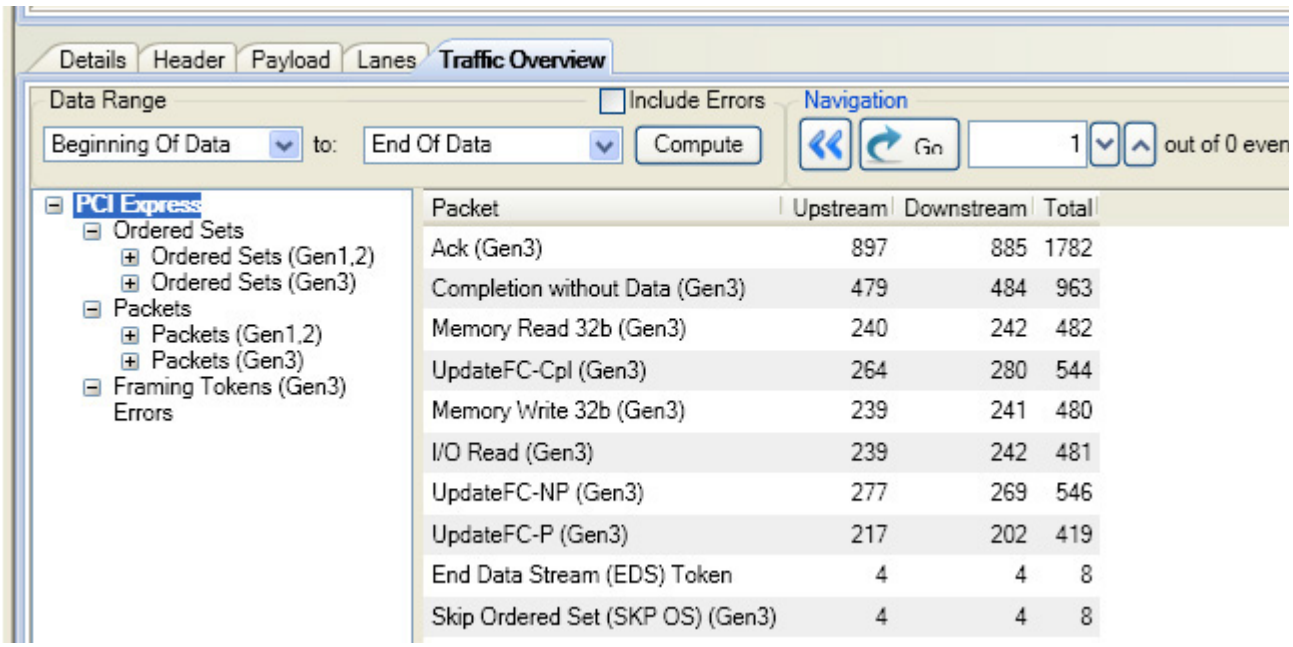
The following screen displays a sample view of the captured PCIe data in the Protocol Viewer window. In this screen, the Lanes tab of the Protocol Viewer window is displayed. The Lanes viewer displays not just the selected packet data across lanes but also the post packet data represented by colors matching the selected packet color in the upper pane.



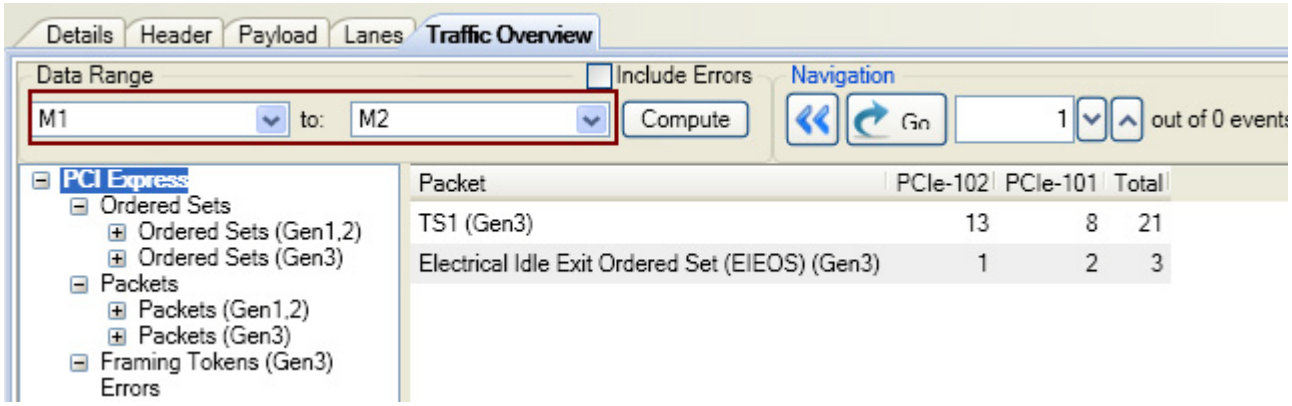
Viewing the captured PCIe Traffic Statistics

You can use the **Traffic Overview** tab in the lower pane of Protocol Viewer to get an overview of the PCIe traffic that is displayed in the upper pane of Protocol Viewer. This tab provides a count of various PCIe packet types captured and displayed in the upper pane. The count of packets is categorized on the basis of packet types.

For each packet type, the count of packets is further segregated based on the direction (upstream or downstream). The following screen displays the traffic statistics in the lower pane. Notice that for each packet type, the count of packets is displayed for upstream as well as downstream direction along with a sum of packets in both directions.



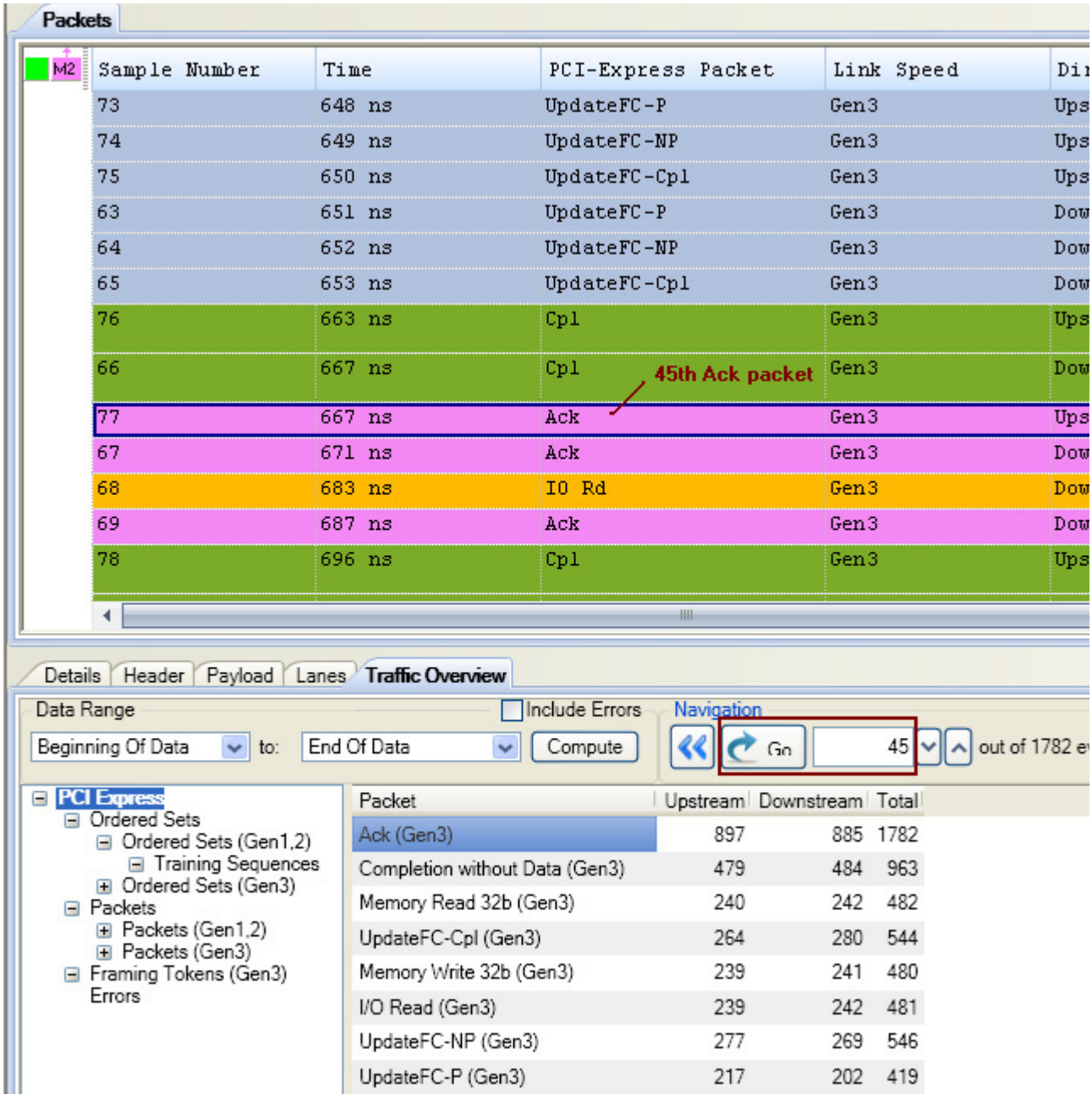
You can specify the data range based on which the traffic statistics get computed in the Traffic Overview tab. For instance, you might want to view the traffic statistics only for the PCIe packets between the markers M1 and M2. In such a situation, you can select M1 as the start point and M2 as the end point in the **Data Range** group box and then click **Compute**. Then Protocol Viewer displays the traffic statistics of only the packets that fall in the specified data range and not for all the PCIe packets displayed in the upper pane. The following screen displays the traffic statistics for the data range starting from M1 and ending at M2 markers.



The Compute button is disabled when U4301A PCIe Analyzer module is capturing data. It becomes enabled when the capture has stopped.

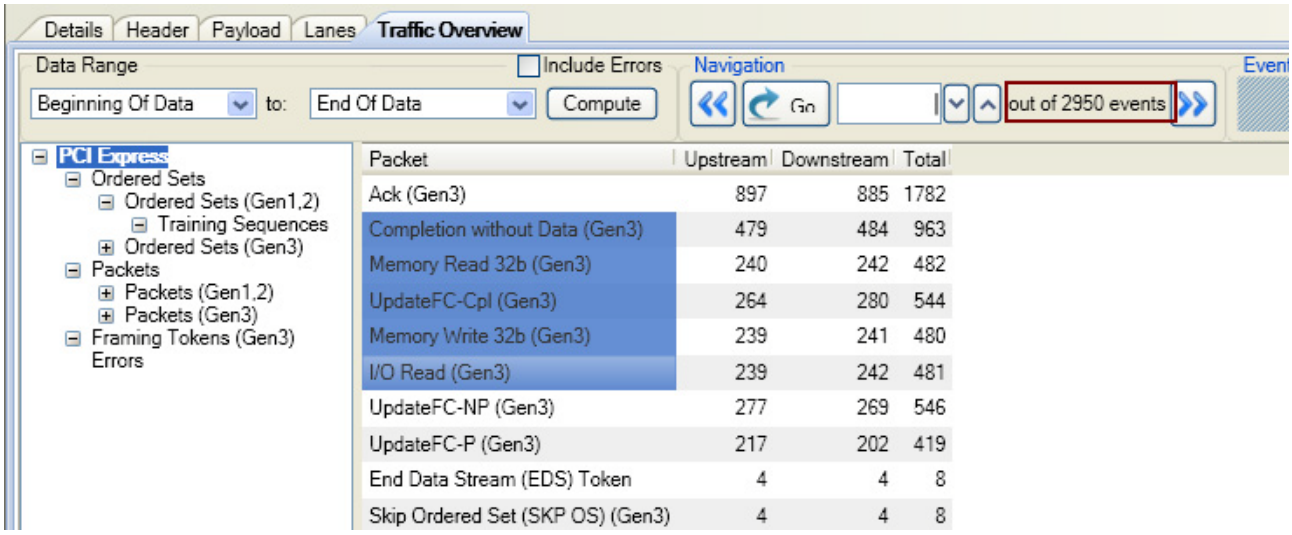
Navigating through the captured PCIe packets

From the displayed traffic overview statistics, you can select a particular packet type and then navigate through the packets displayed in the upper pane for that packet type. For instance, there are total 1782 packets of the type Ack and you want to view the details of the 45th Ack packet out of these 1782 Ack packets. To go directly to the 45th Ack packet out of the total Ack packets, you can select this packet type in the Traffic Overview results and then type 45 in the Navigation text box and click Go. This takes you directly to the 45th Ack packet in the upper pane of Protocol Viewer.



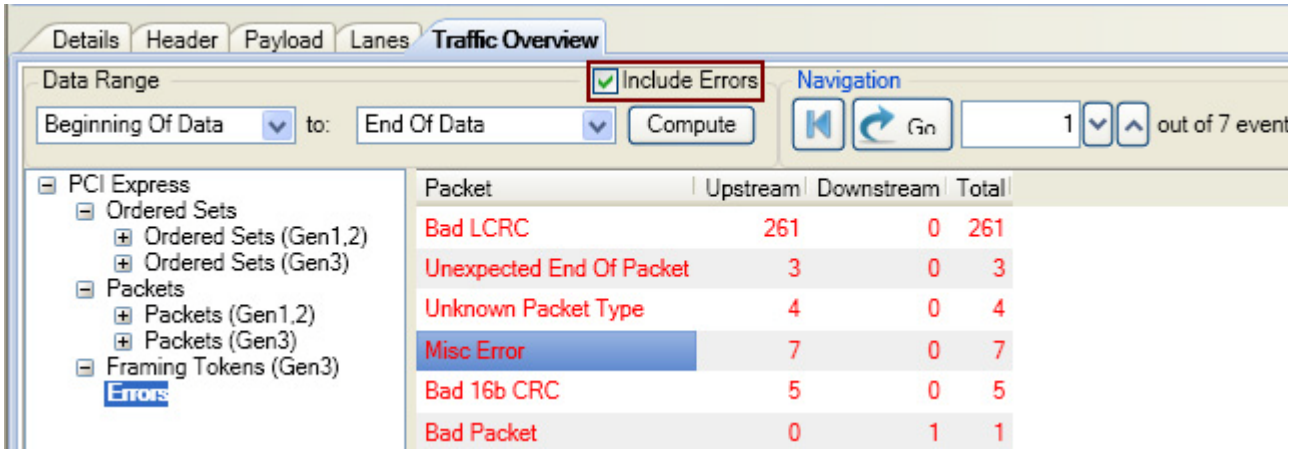
You can also navigate through the PCIe packets of a particular direction (upstream or downstream). To do this, select a particular packet type in the displayed traffic statistics and then select the count column for the required direction. Then specify the packet number in the Navigation text box to reach directly to that packet.

You can also select multiple packet types in the Traffic Overview tab by clicking a packet type and then dragging the mouse over to the other packet types that you want to select. When you select multiple packet types, the Navigation section displays the total packet count for all the selected packet types.



Viewing Errored Packets Statistics

If you want to include the count of errored packets in the traffic overview, then select the Include Errors check box. You can then click the Errors option in the left panel of Traffic Overview tab. This displays the count of errored packets categorized based on different error types and direction.



Exporting Captured PCIe Data to a .csv File

You can export the captured PCIe packet information from the Protocol Viewer window to a specified .csv file and use it later in other analysis tools. You do this by clicking the csv toolbar button in the Protocol Viewer window. On clicking this toolbar button, the **Protocol Export** dialog box is displayed in which you can specify the details of export such as the range of packet data that you want to export and the delimiter that you want to use to delimit the exported data in the specified .csv file.

For details on how to export data to a .csv file, click the Help button in the Protocol Export dialog box.

Glossary

D

DUT Device Under Test.

I

interposer Describes a probing method where the probe is located between a slot and the PCI Express device under test.

M

midbus probe Describes a probing method where Soft Touch footprints are designed into a DUT board between the controller and the device under test.

10 Glossary

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